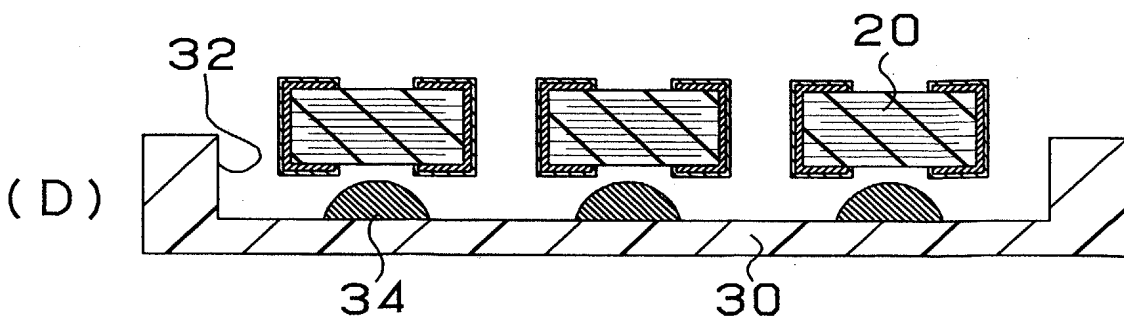
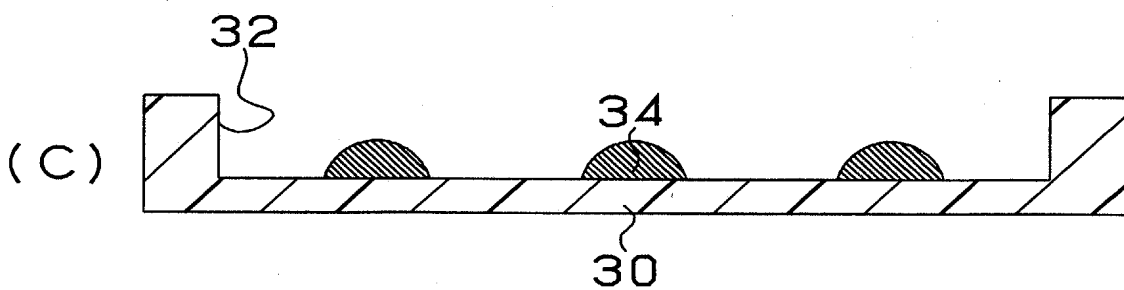
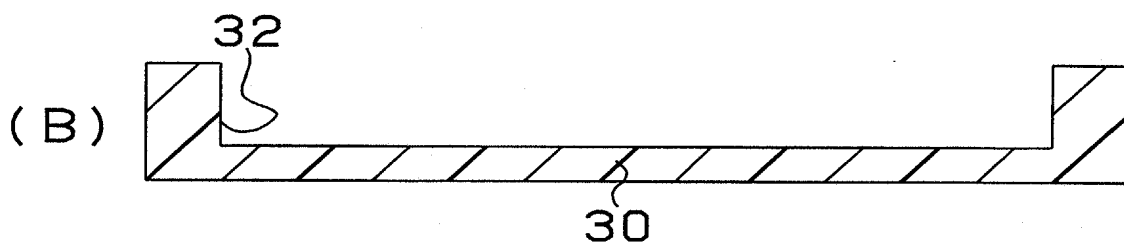
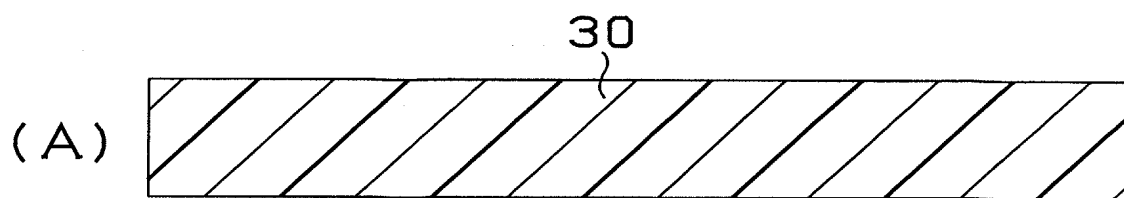
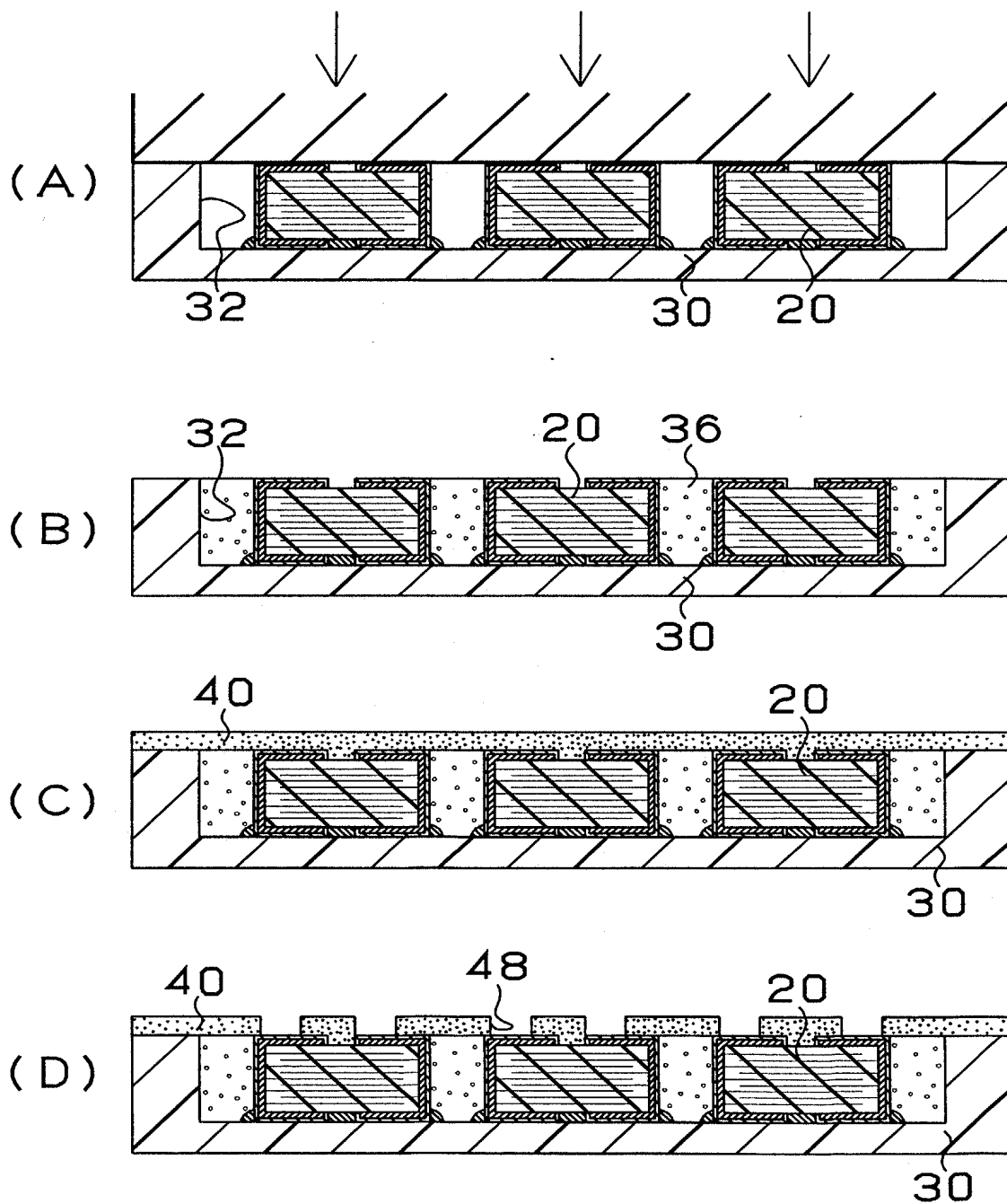
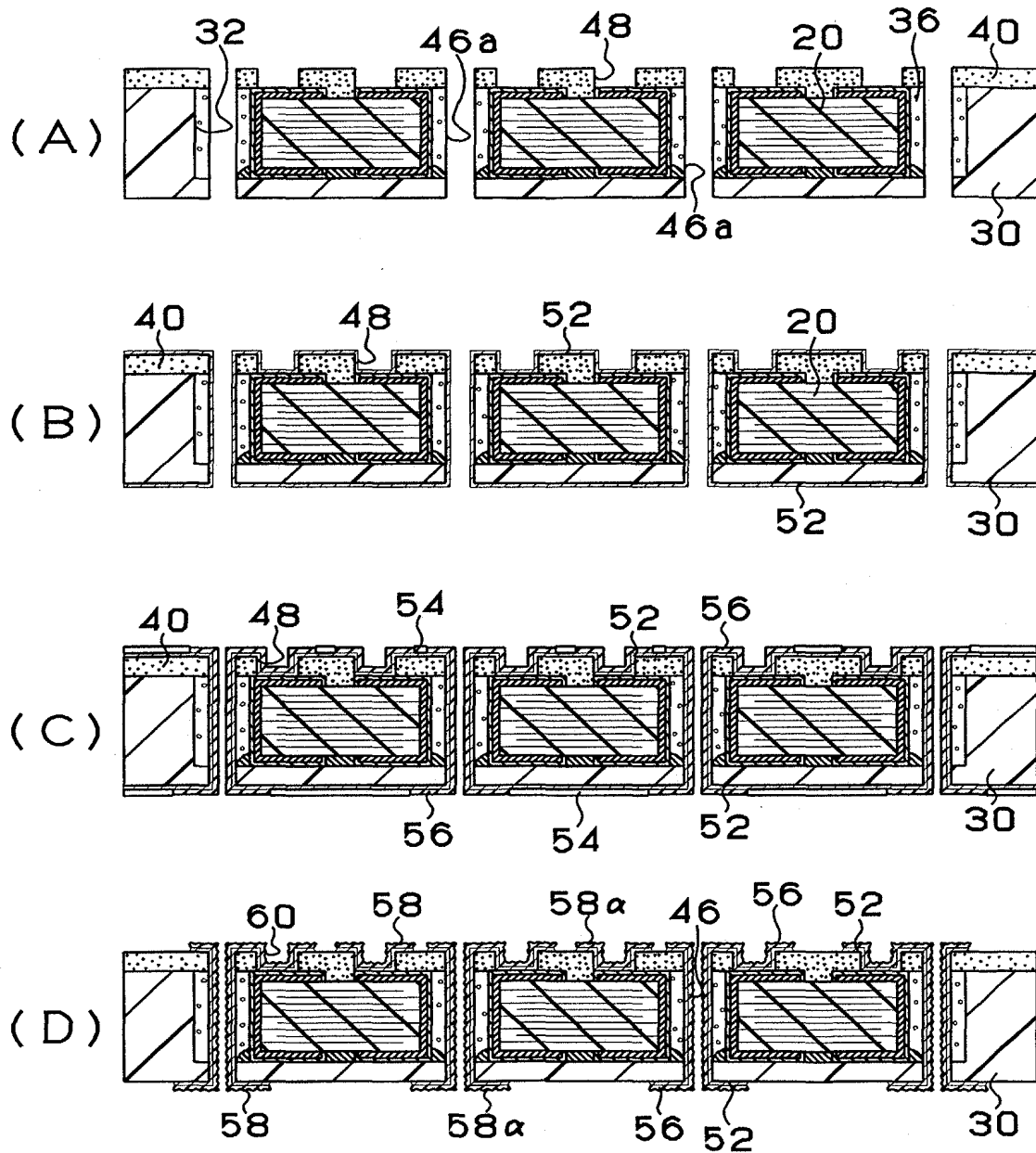
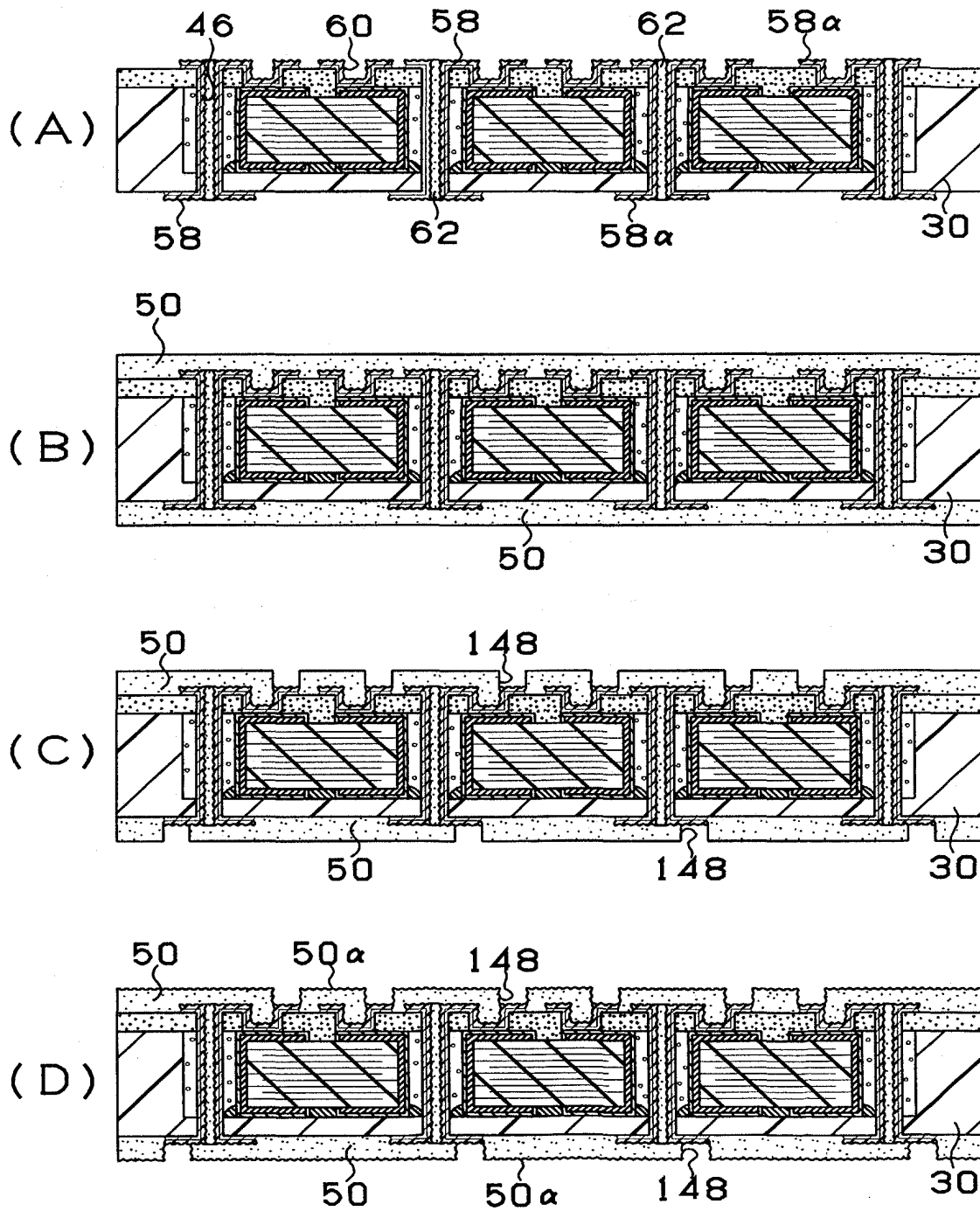


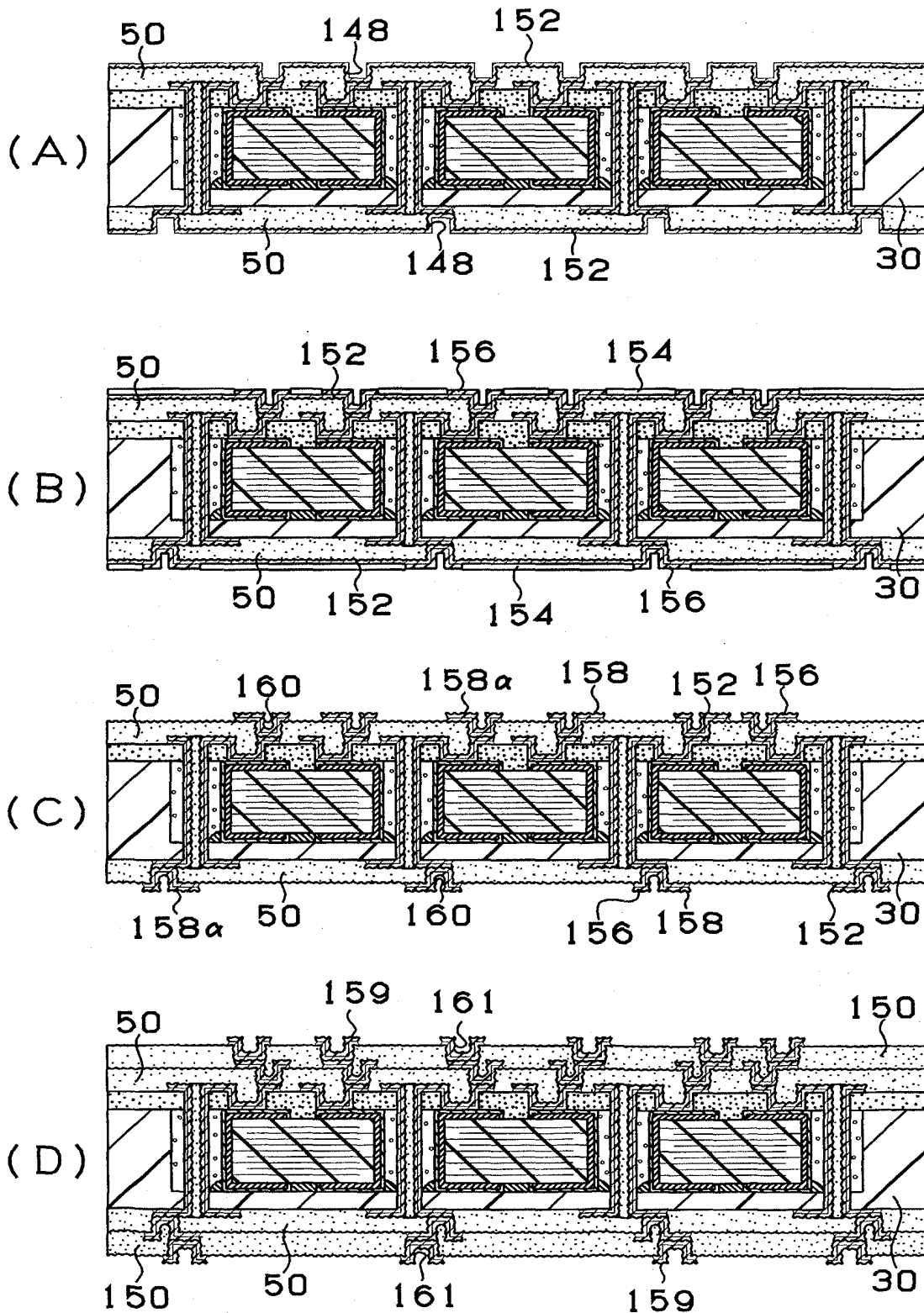
1/73  
Fig. 1



2/73  
Fig. 2

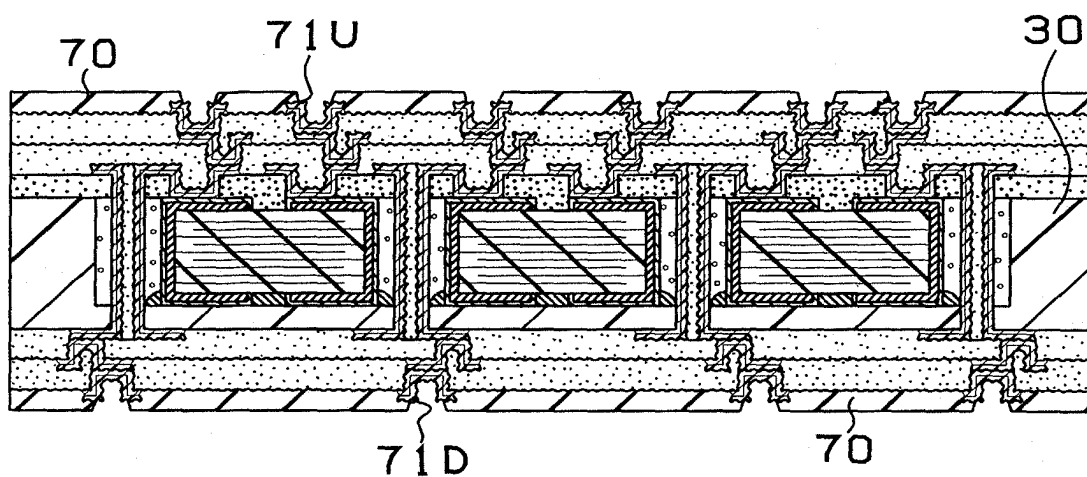
3/73  
Fig. 3

4/73  
Fig. 4

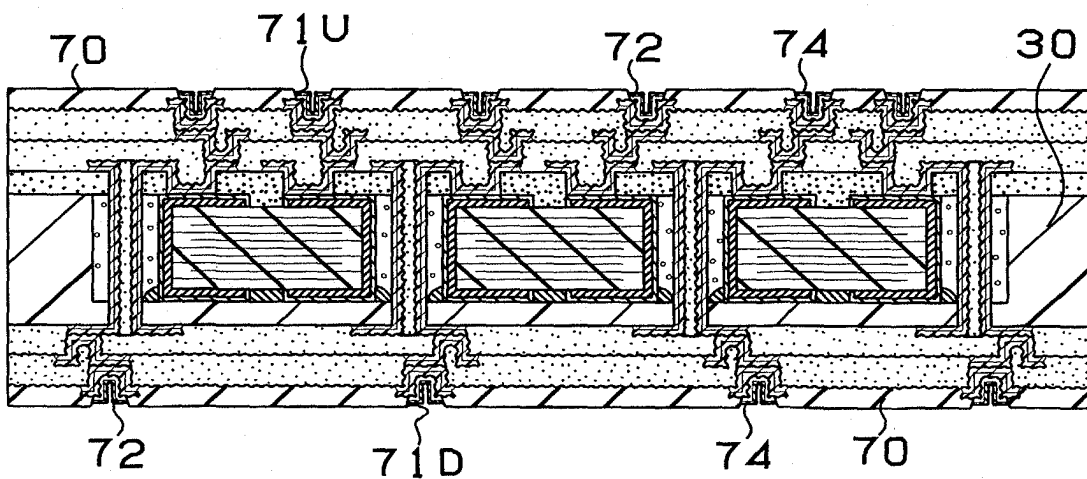
5/73  
Fig. 5

6/73  
Fig. 6

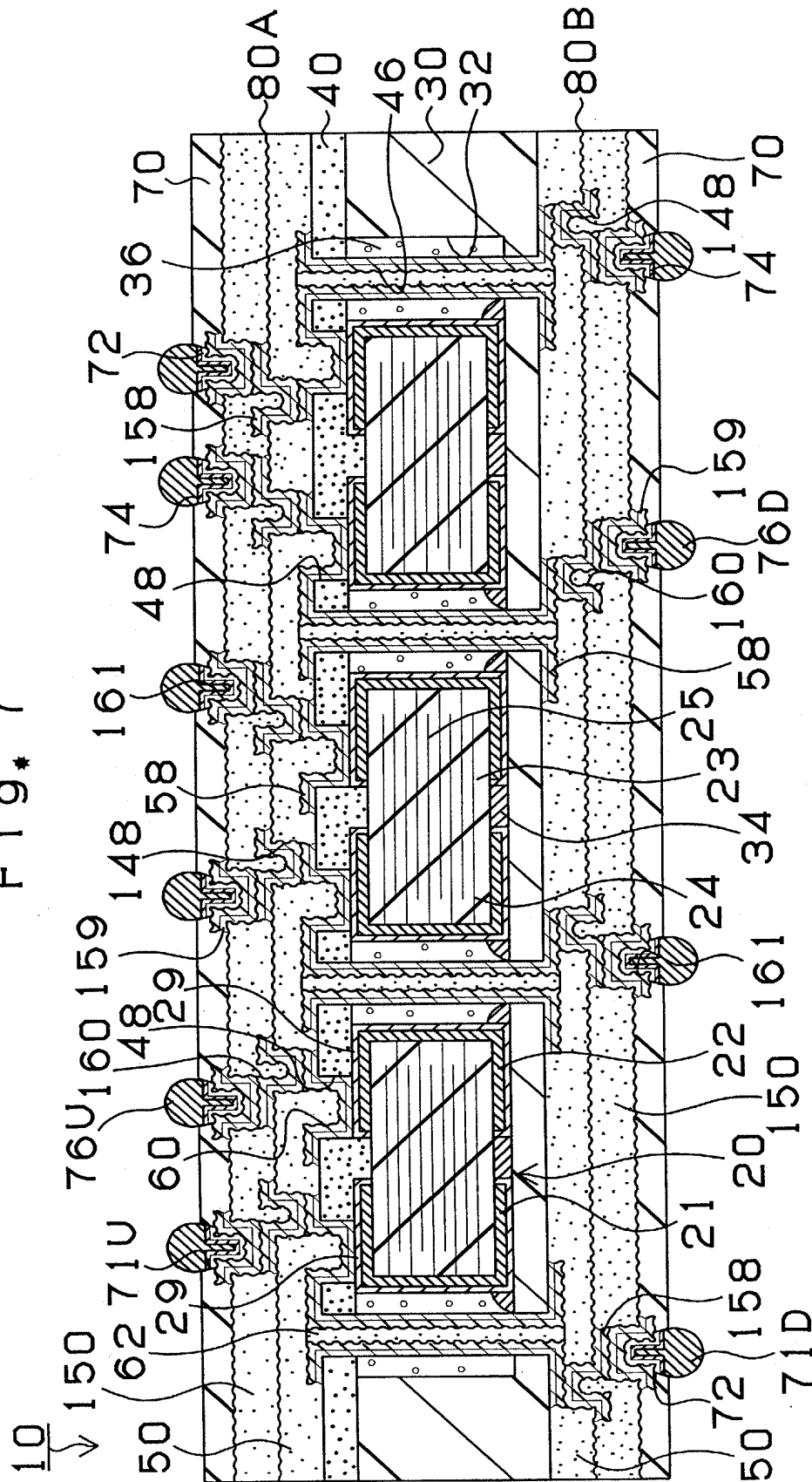
(A)



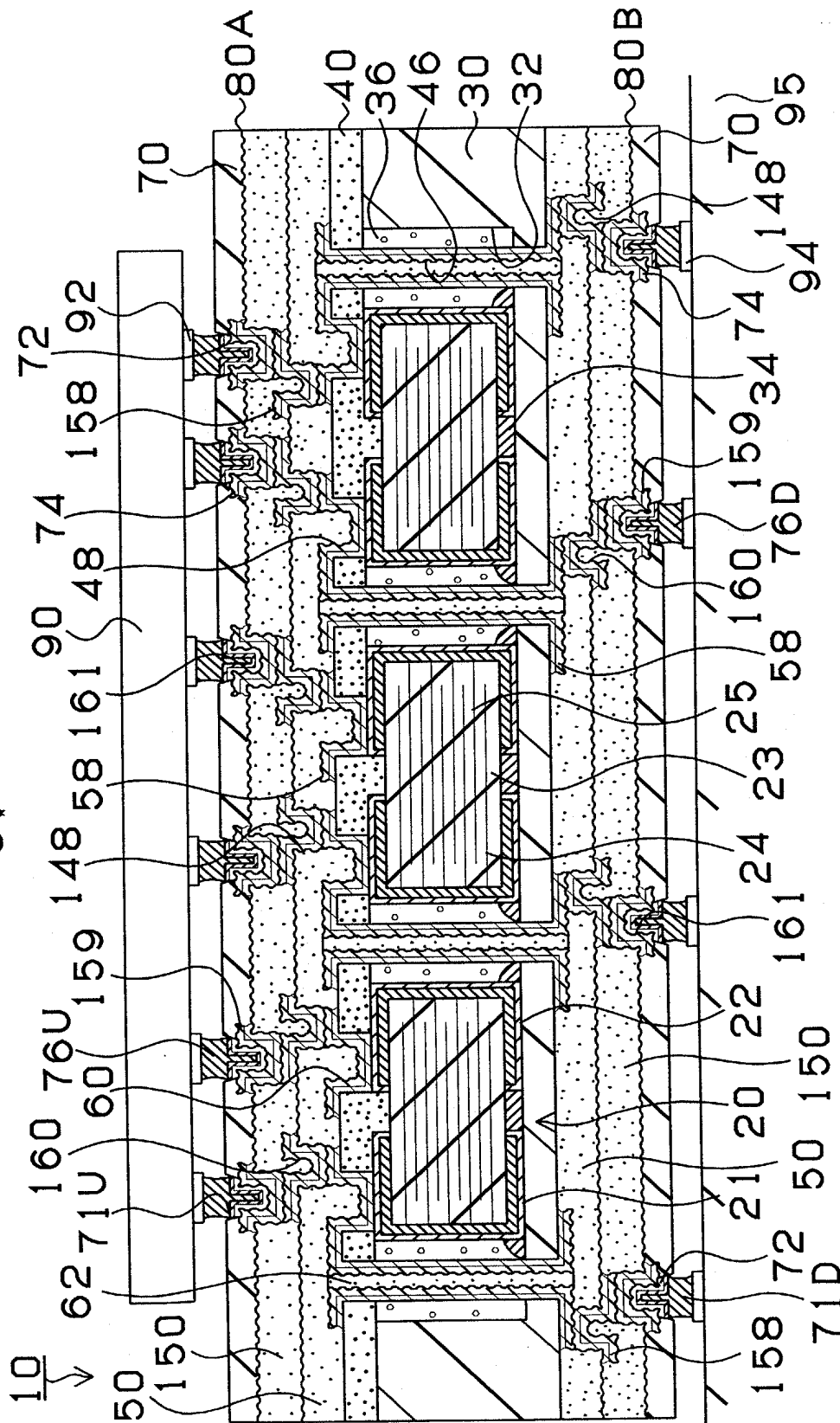
(B)



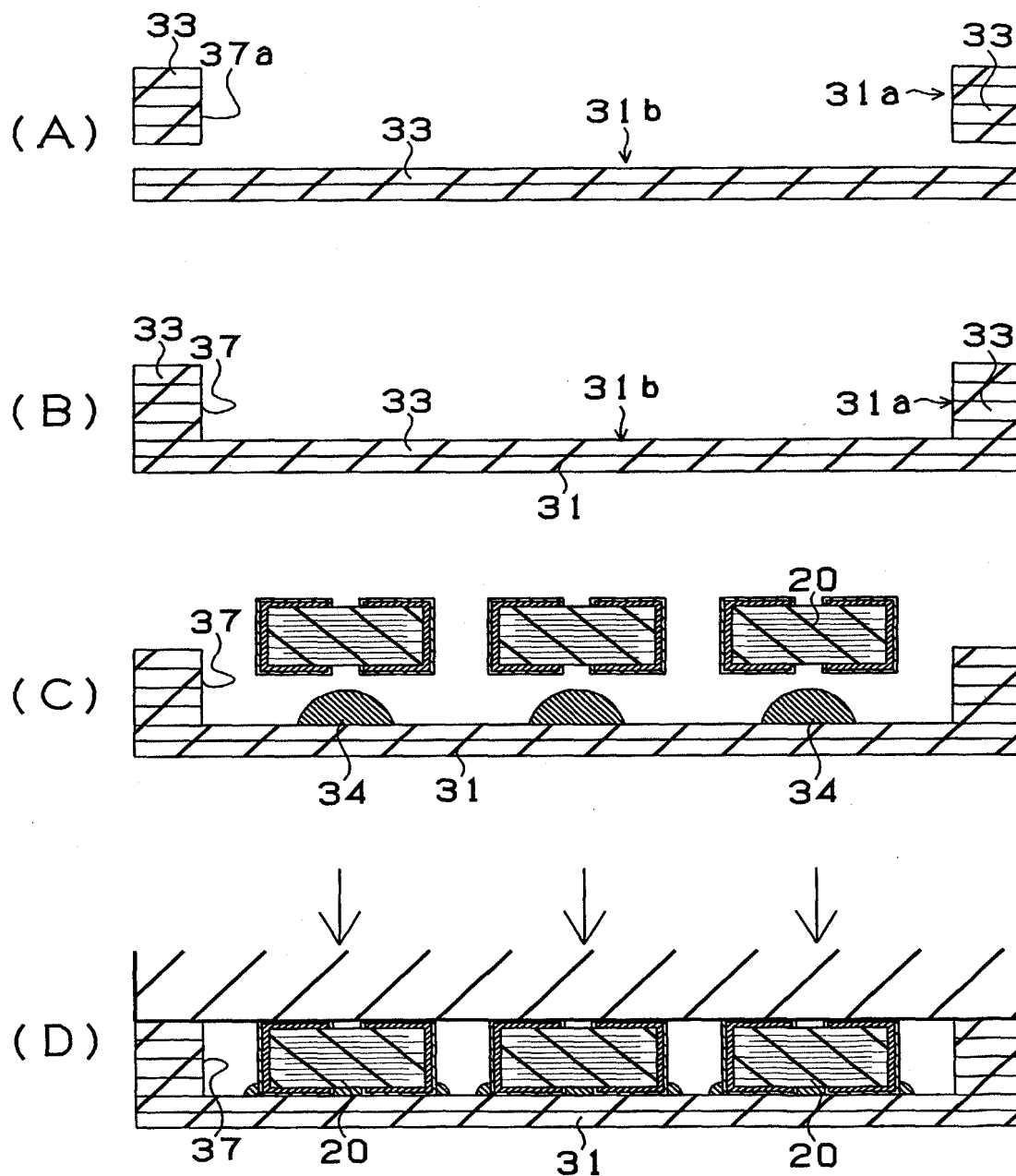
7/737  
Fig.\*

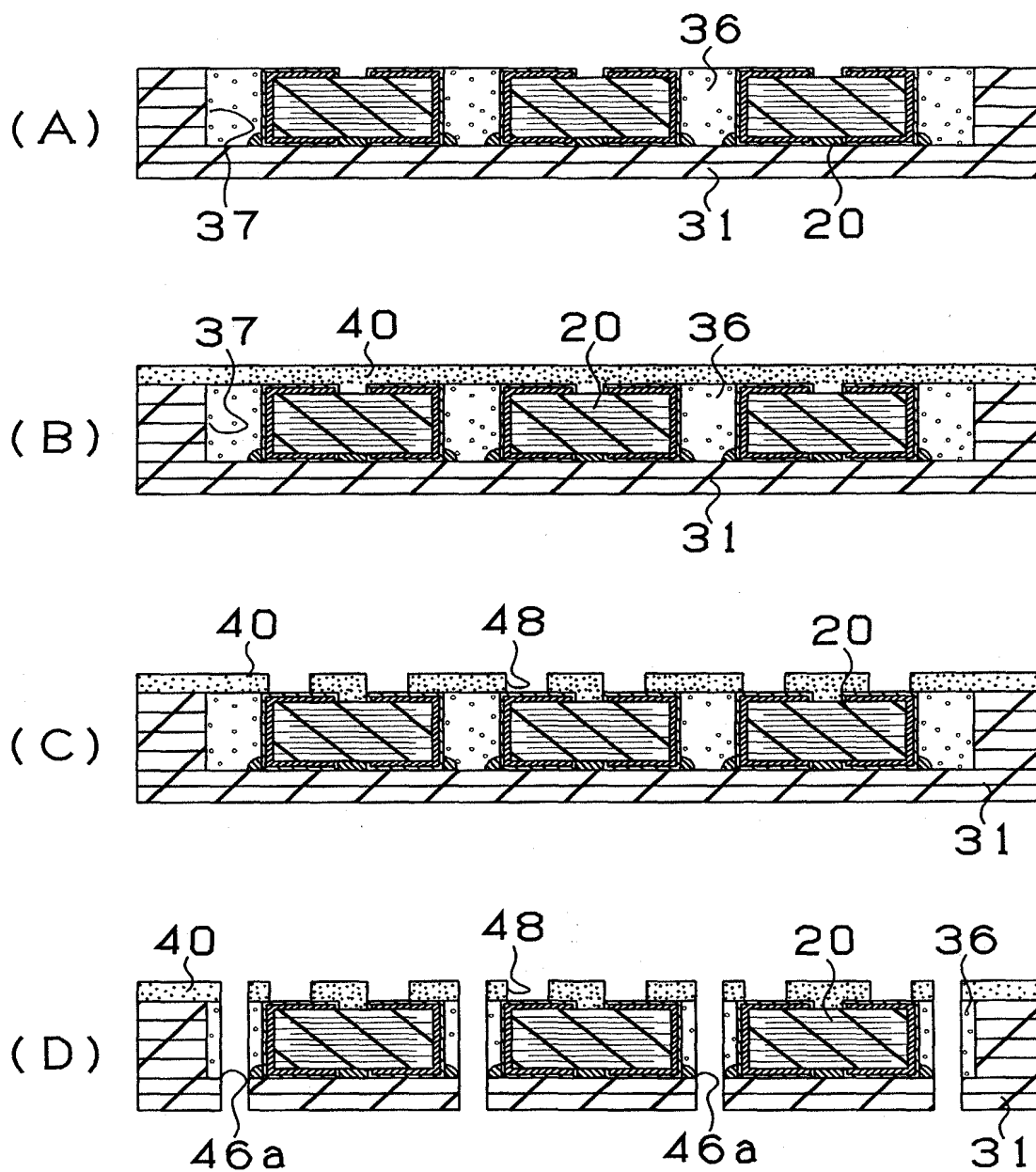


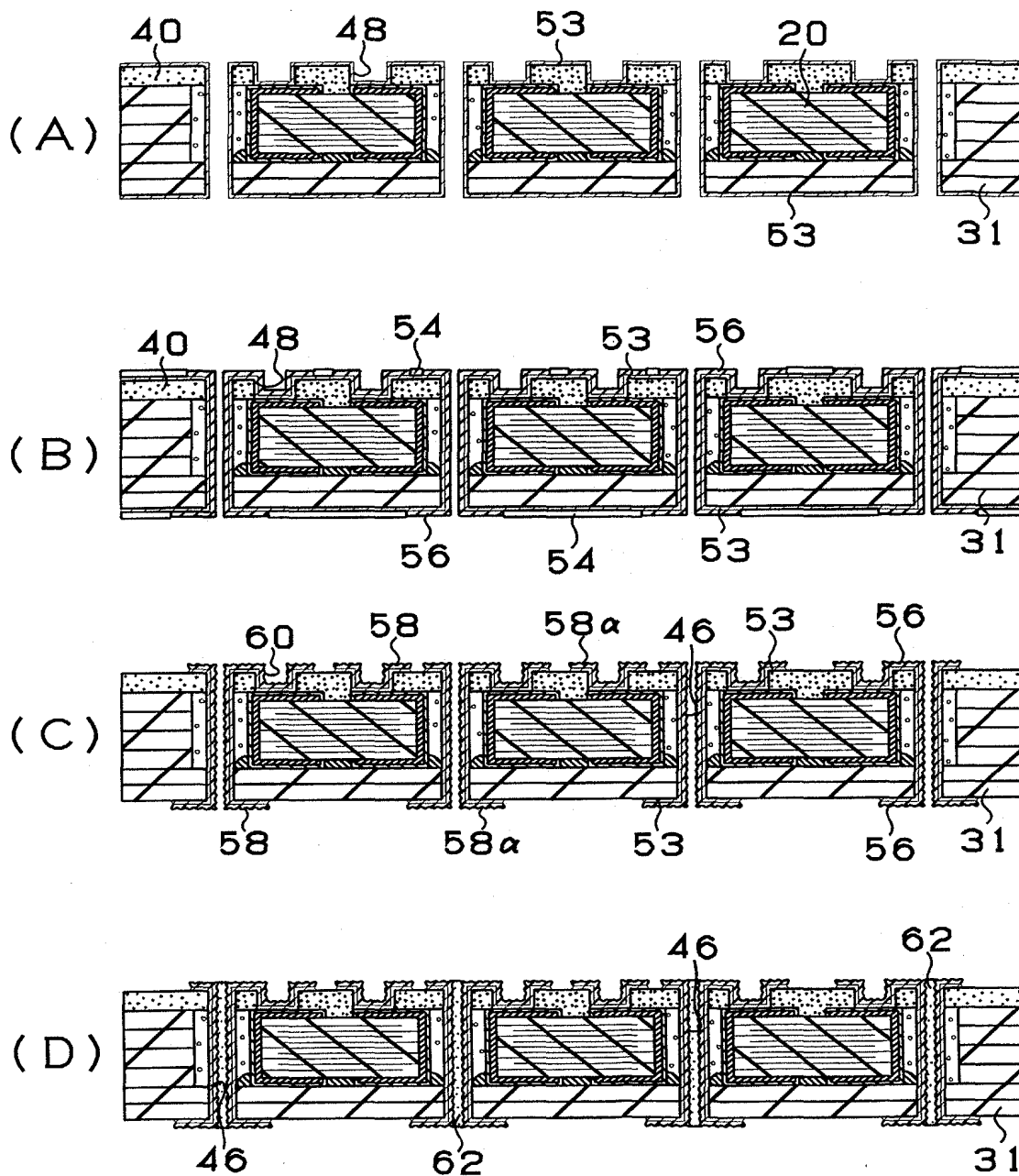
8/73  
Fig. 8

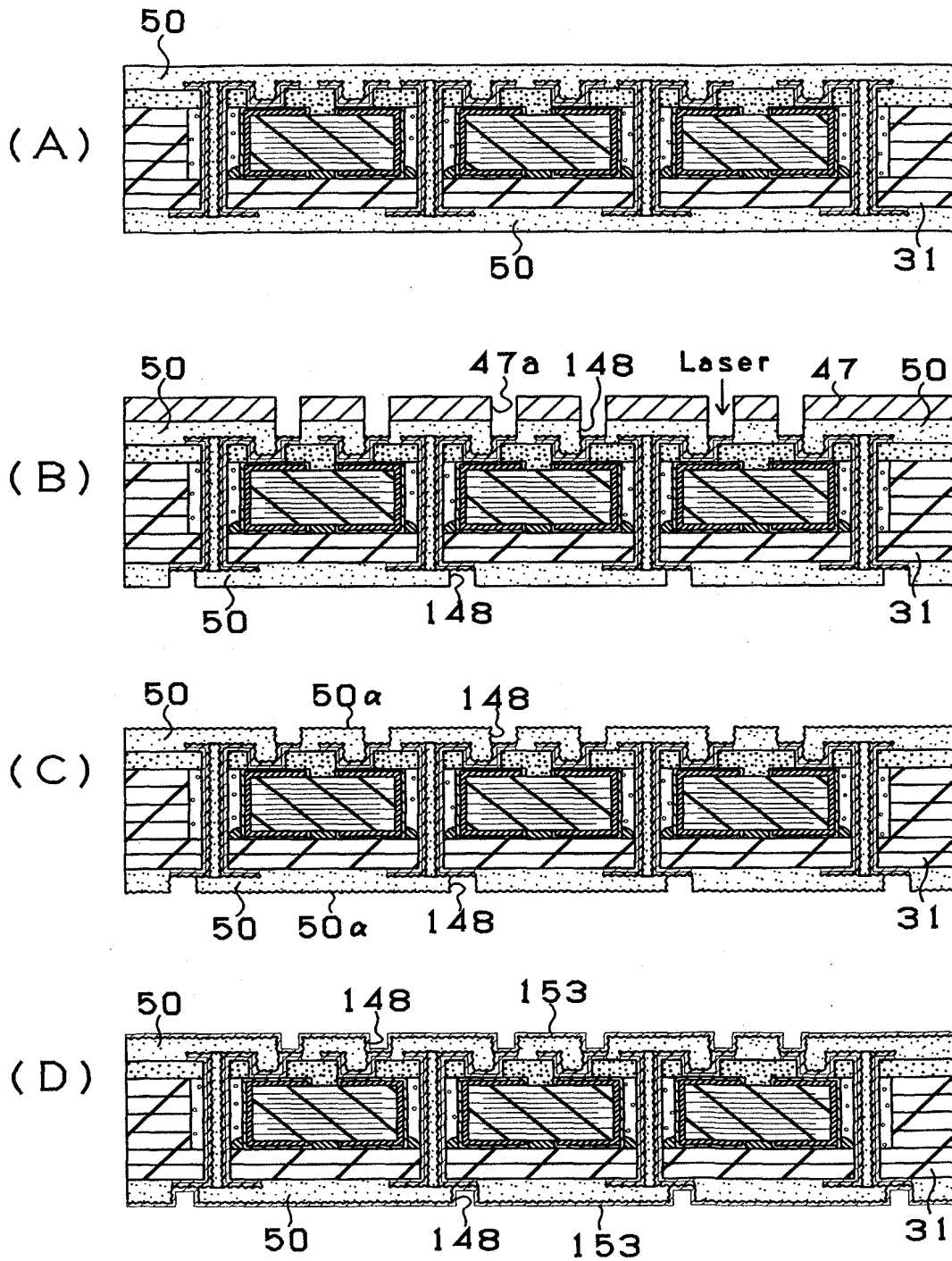


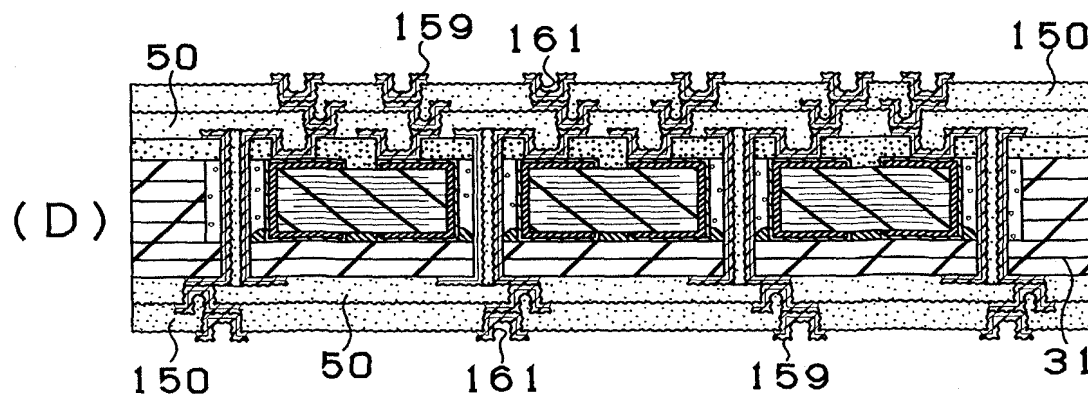
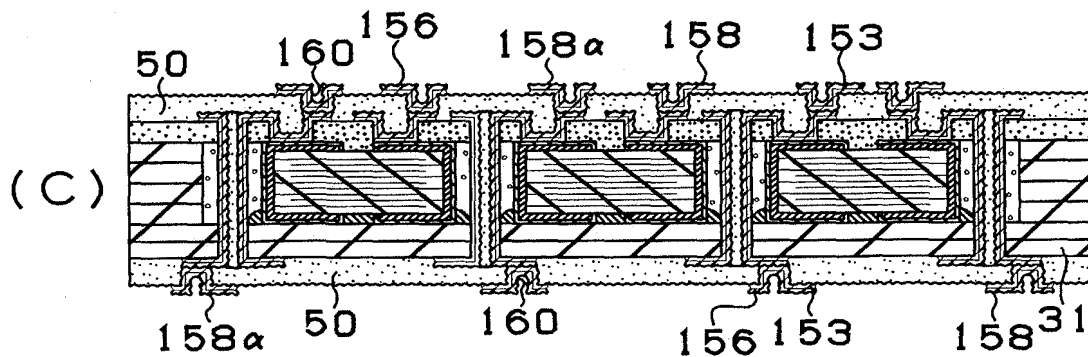
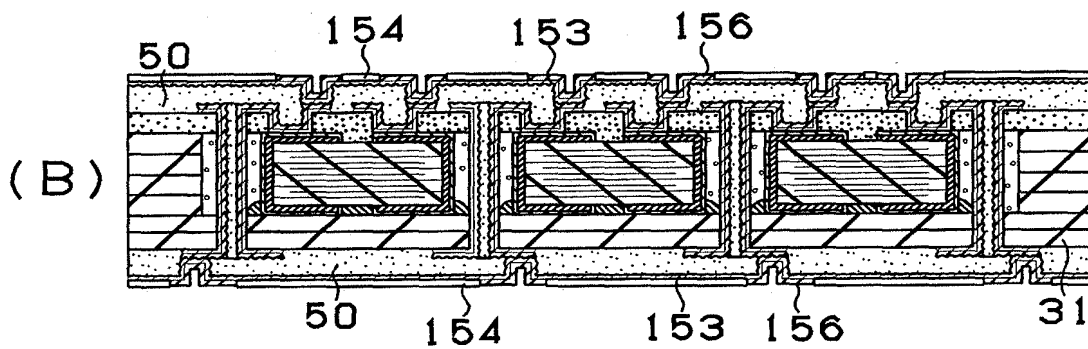
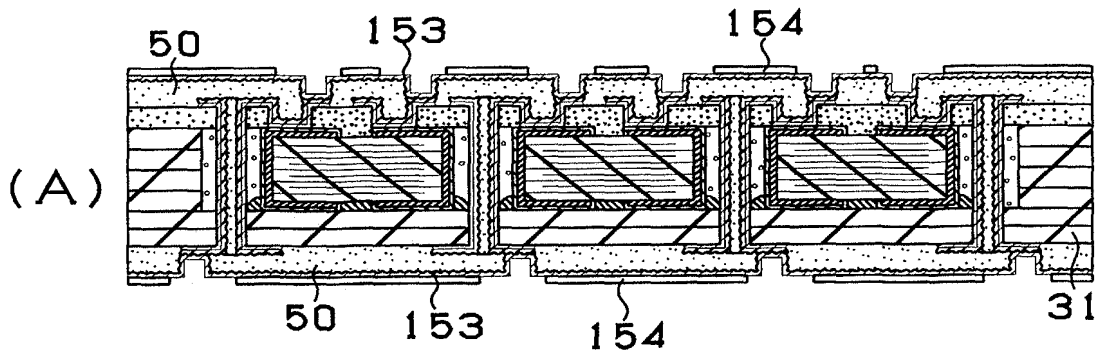


9/73  
Fig. 9

10/73  
Fig. 10

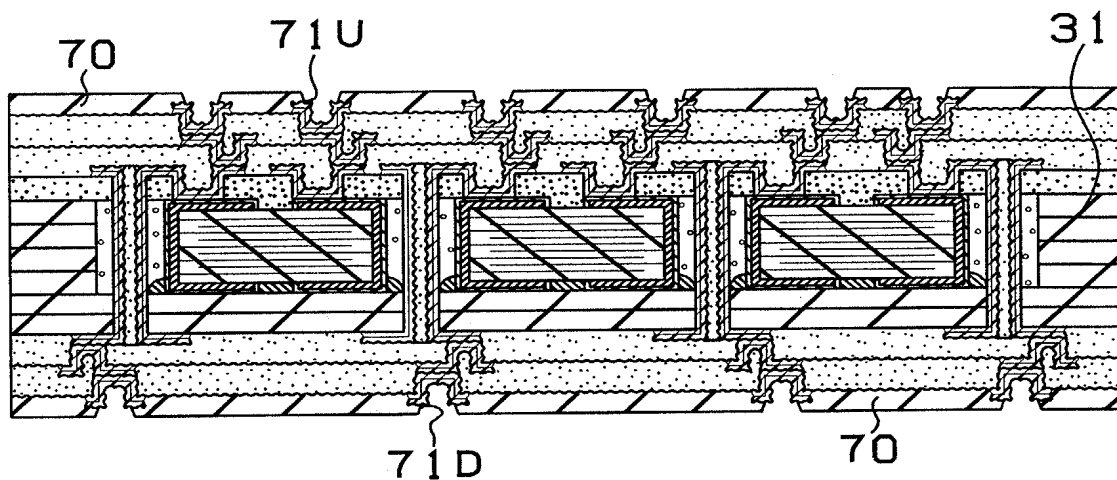
11/73  
Fig. 11

12/73  
Fig. 12

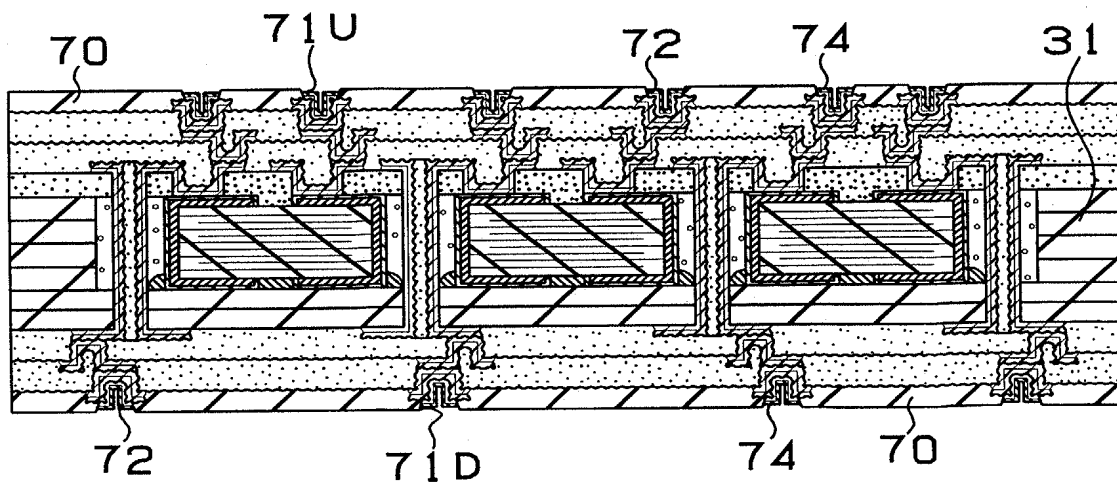
13/73  
Fig. 13

14/73  
Fig. 14

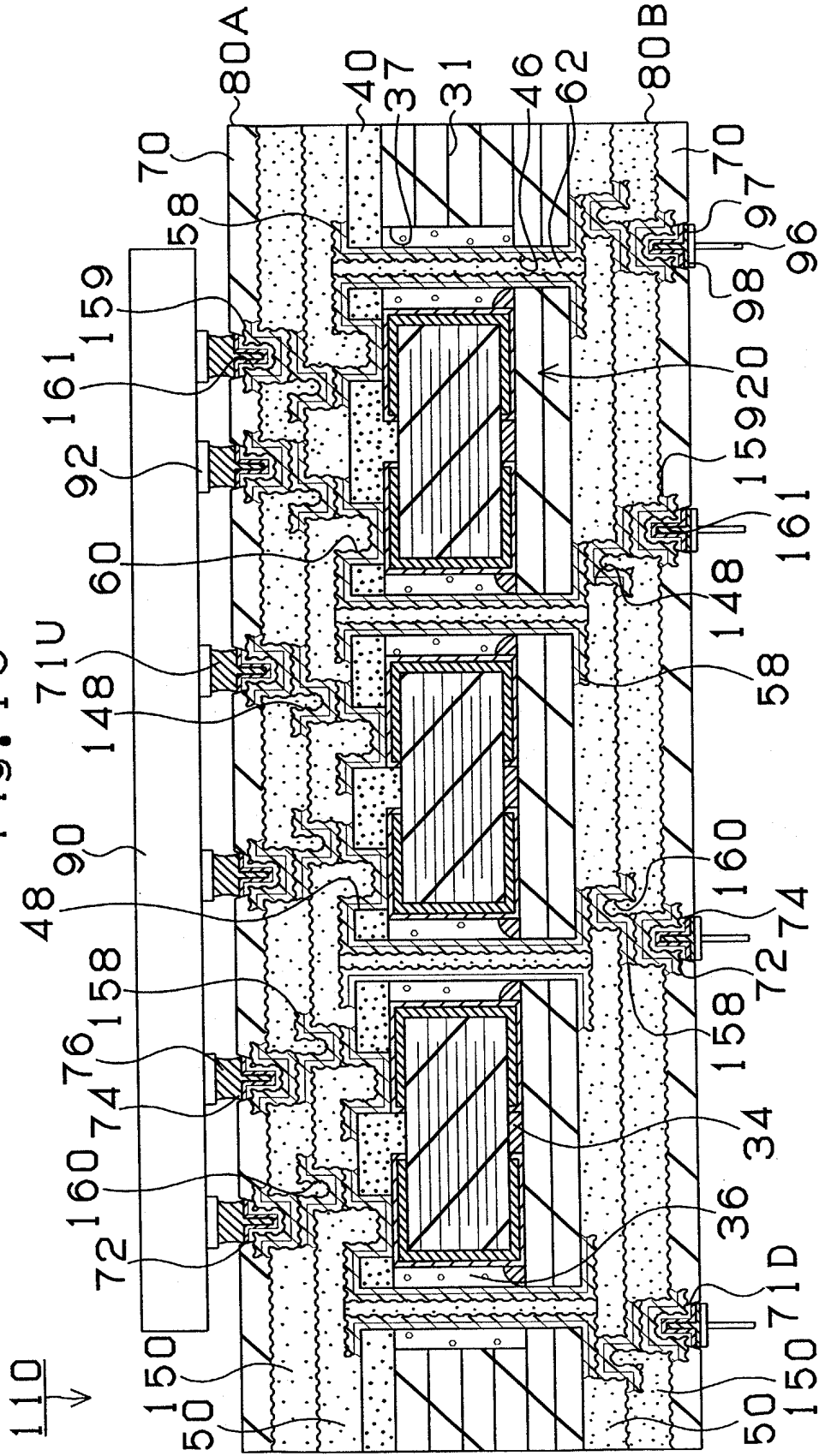
(A)

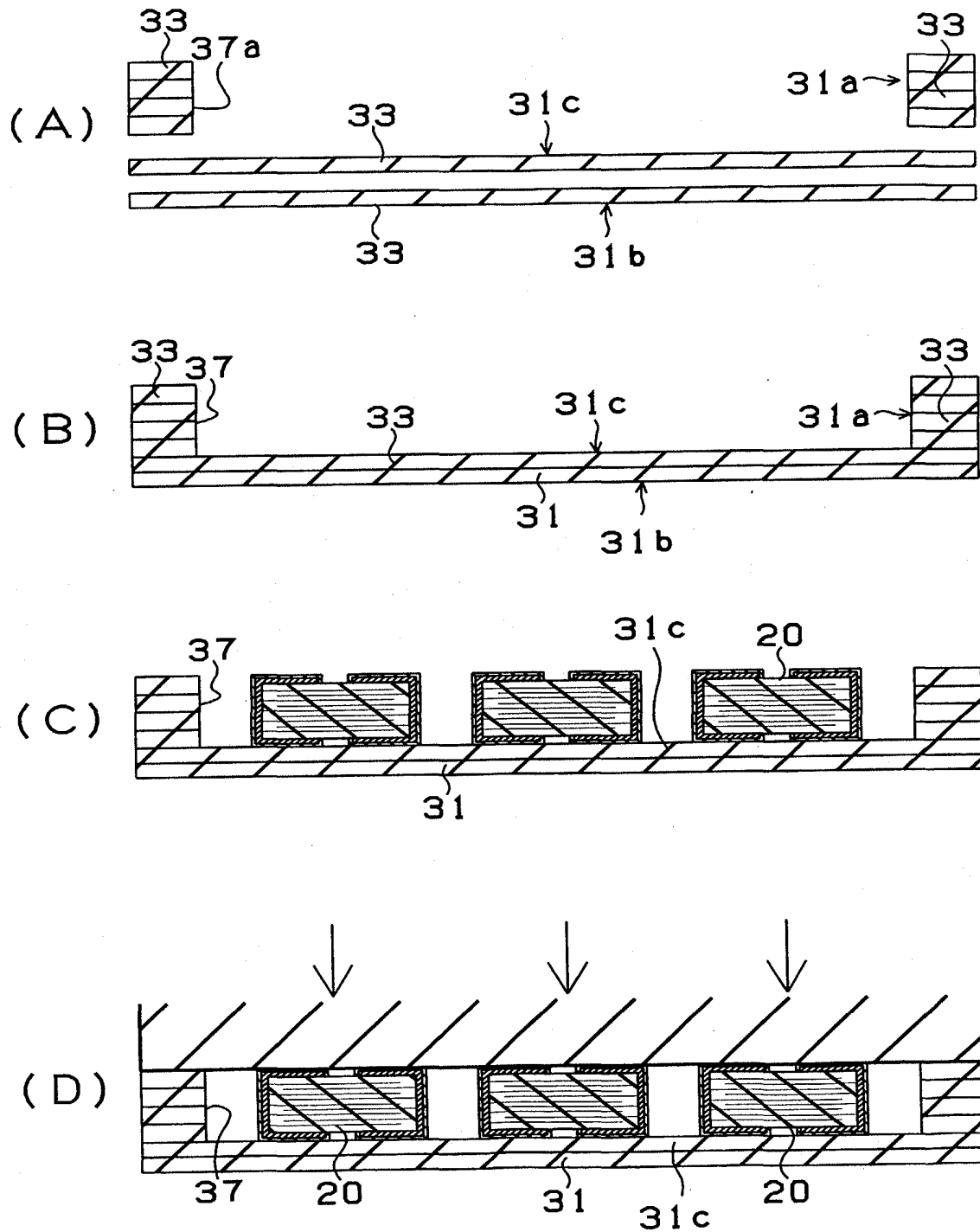


(B)



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Fig. 15

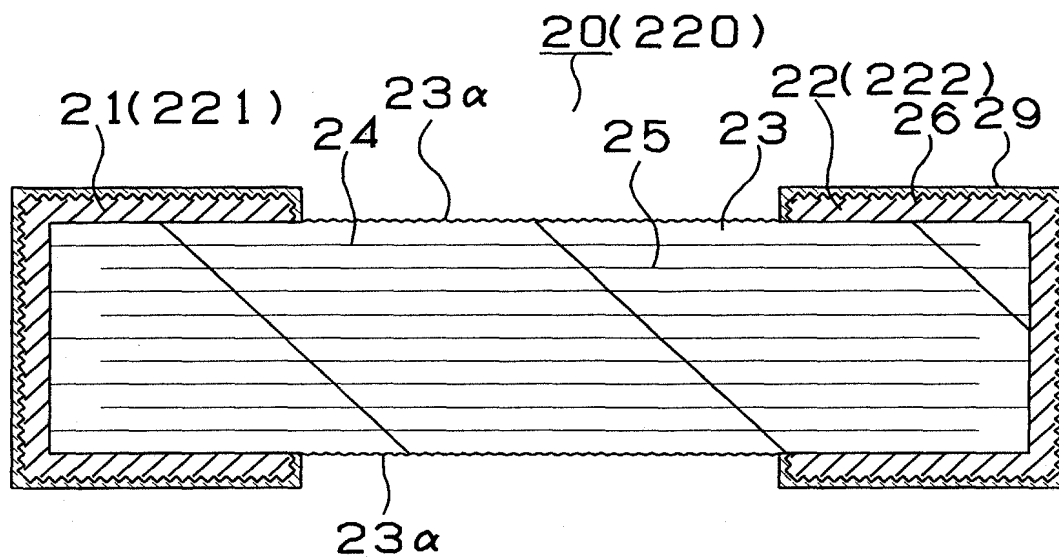


16/73  
Fig. 16

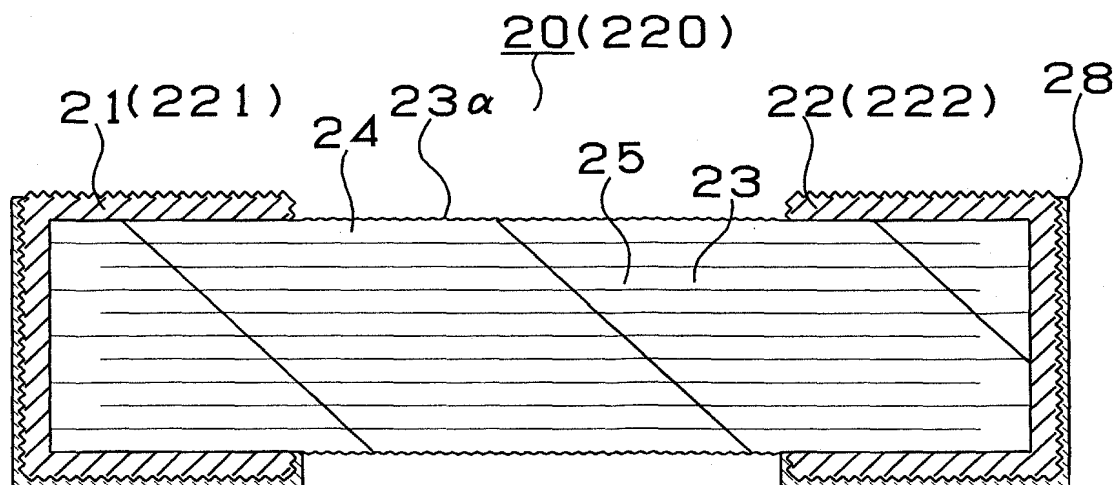


17/73  
Fig. 17

(A)

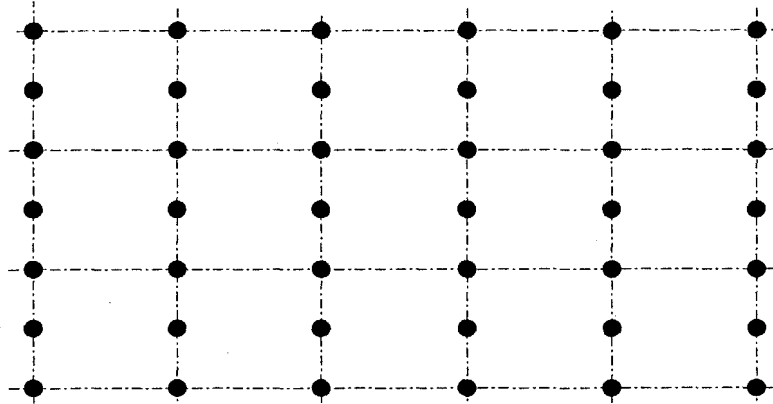


(B)

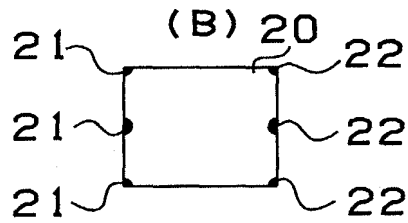


18/73  
Fig. 18

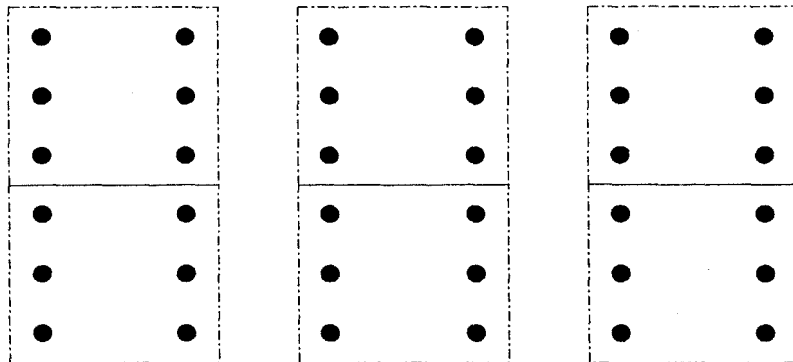
(A)



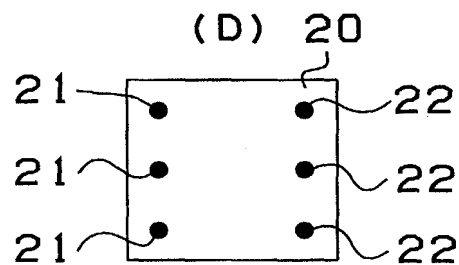
(B)

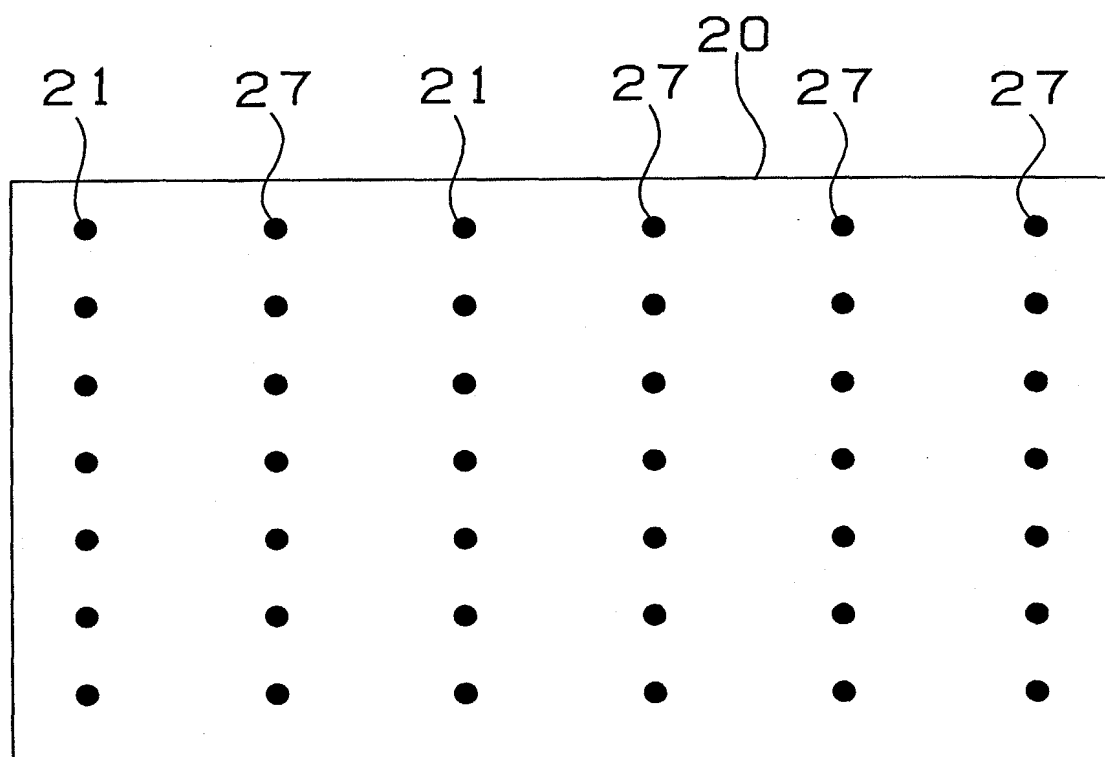


(C)



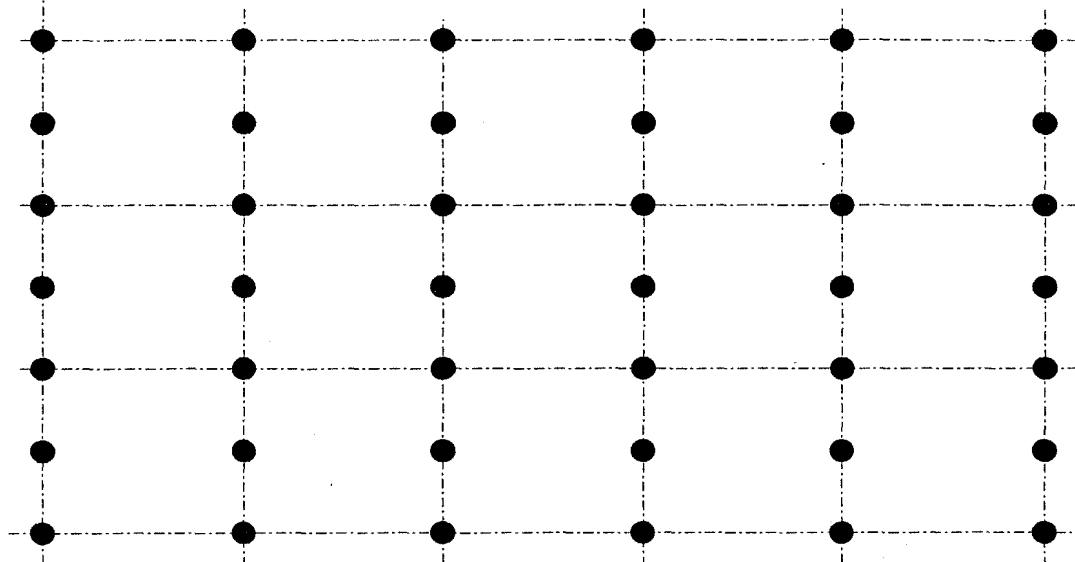
(D)



19/73  
Fig. 19

20/73  
Fig. 20

(A)



(B)

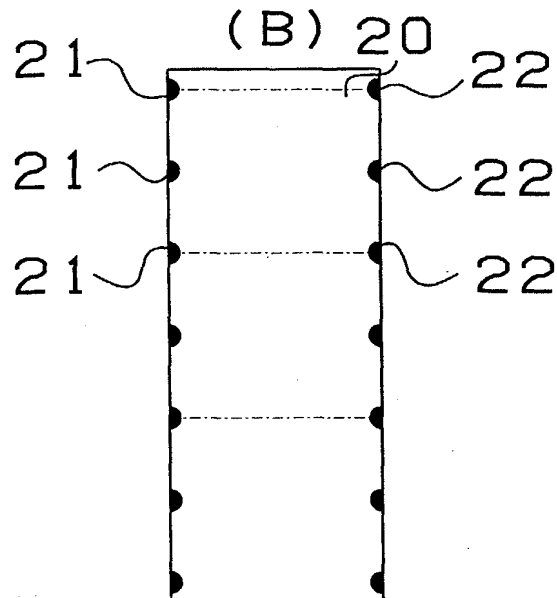
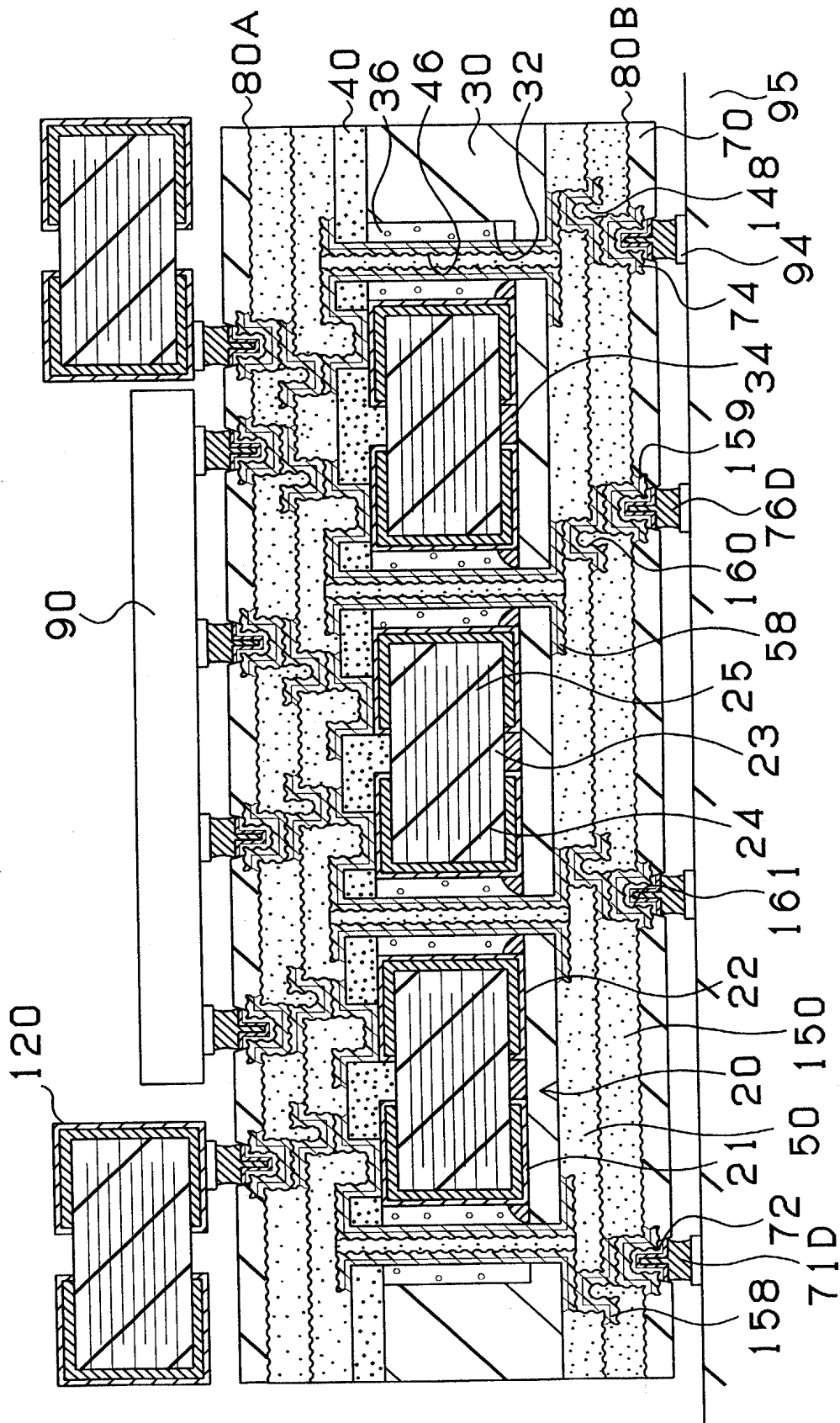
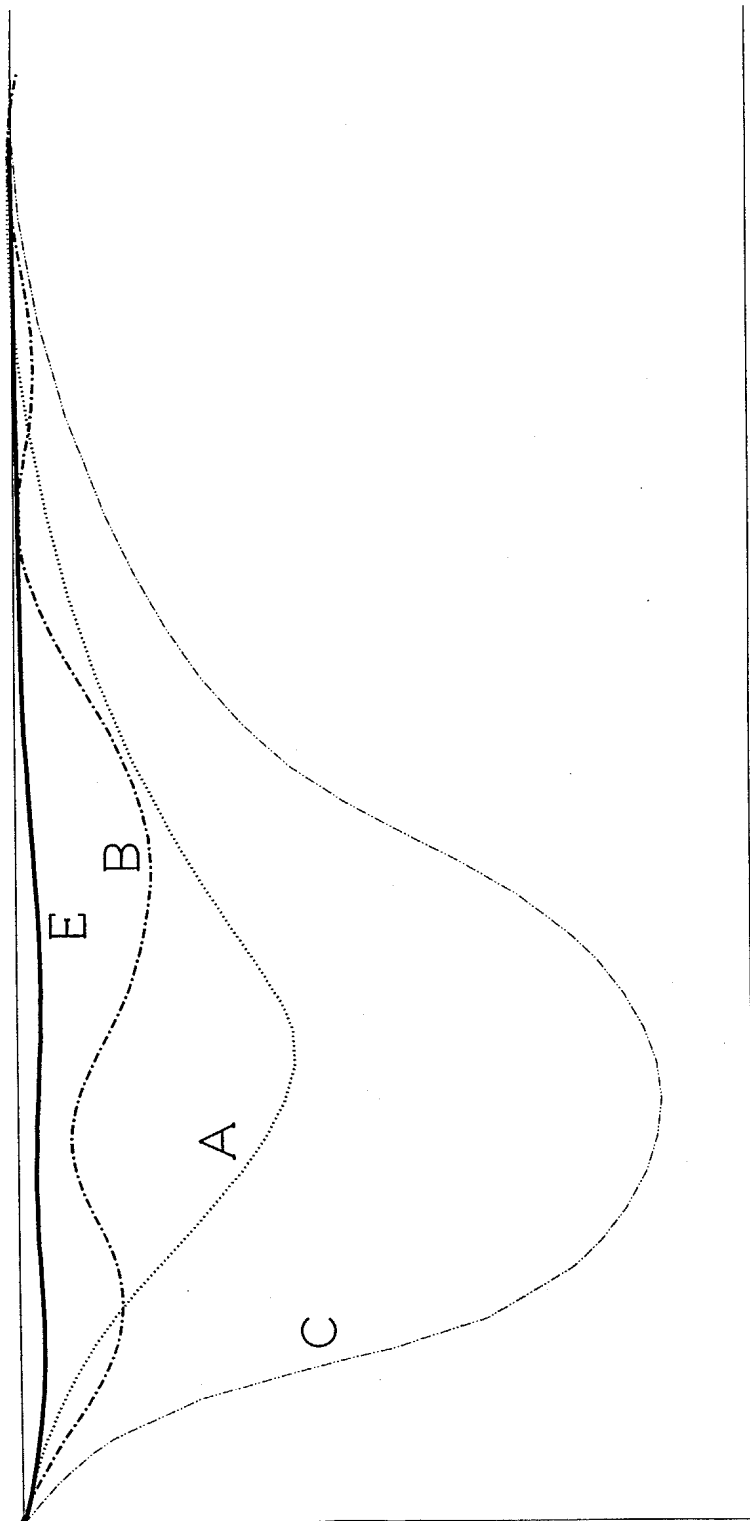


Fig. 21



22/73  
Fig. 22

Voltage



Time

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23/73  
FIG. 23

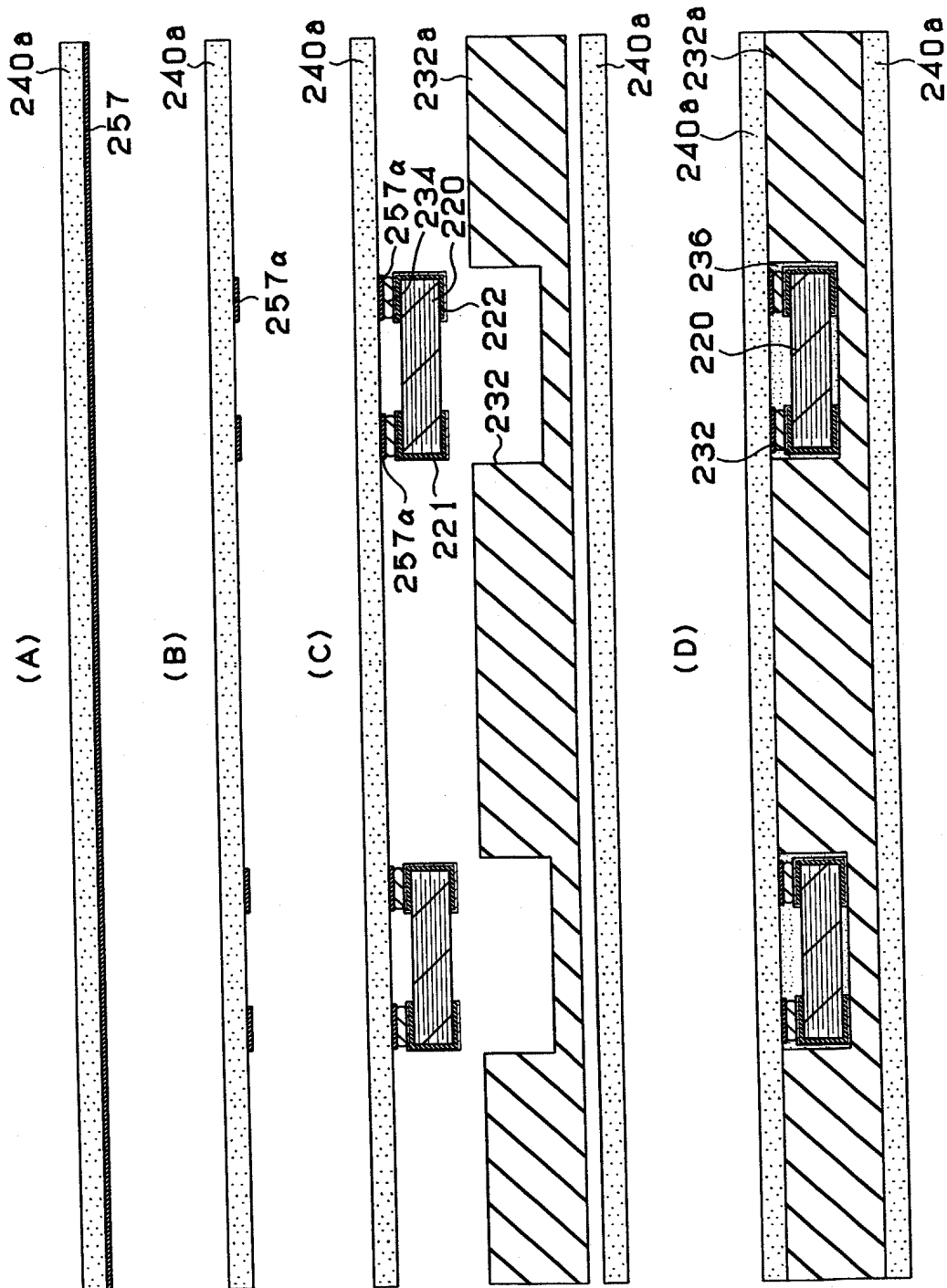
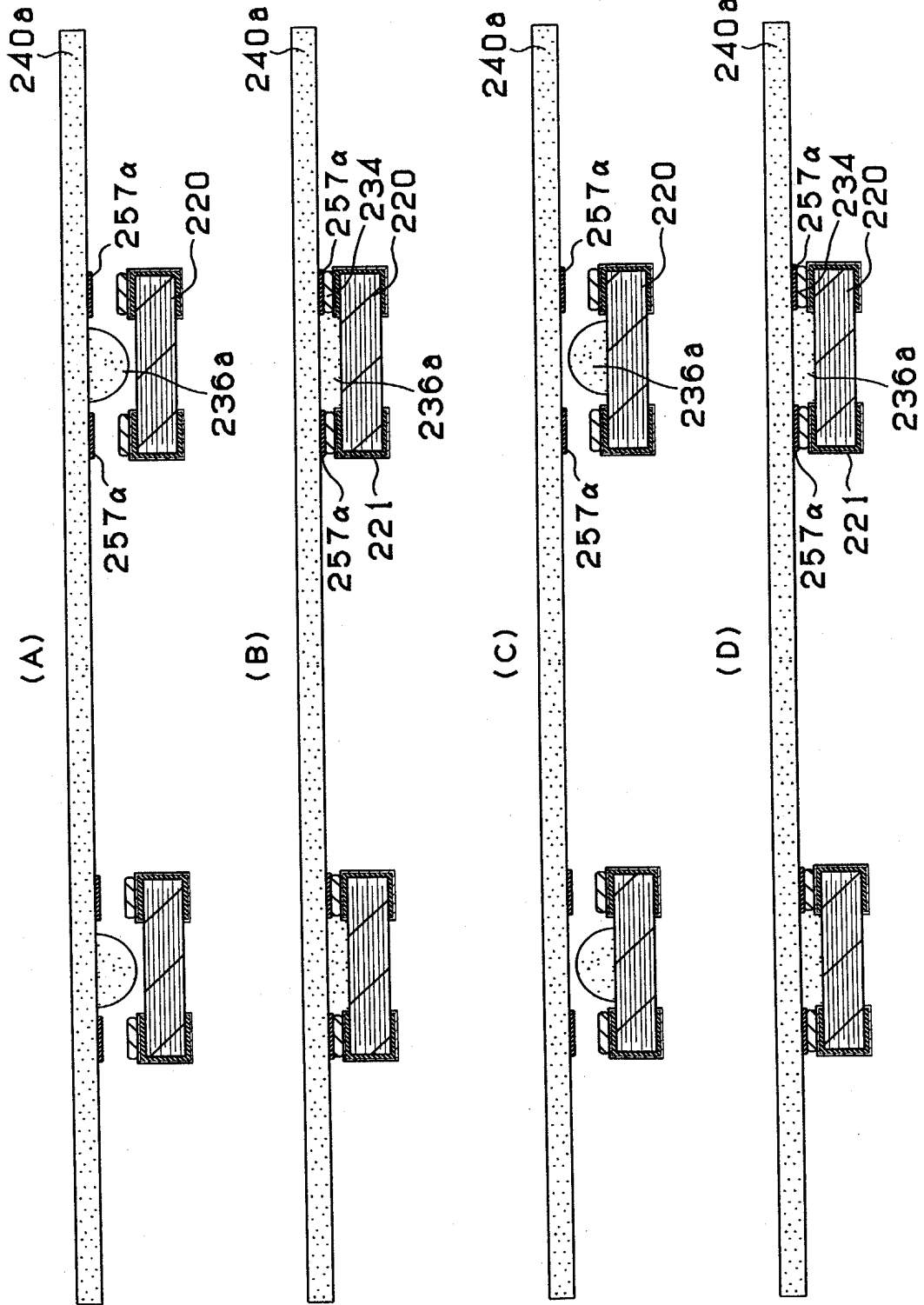
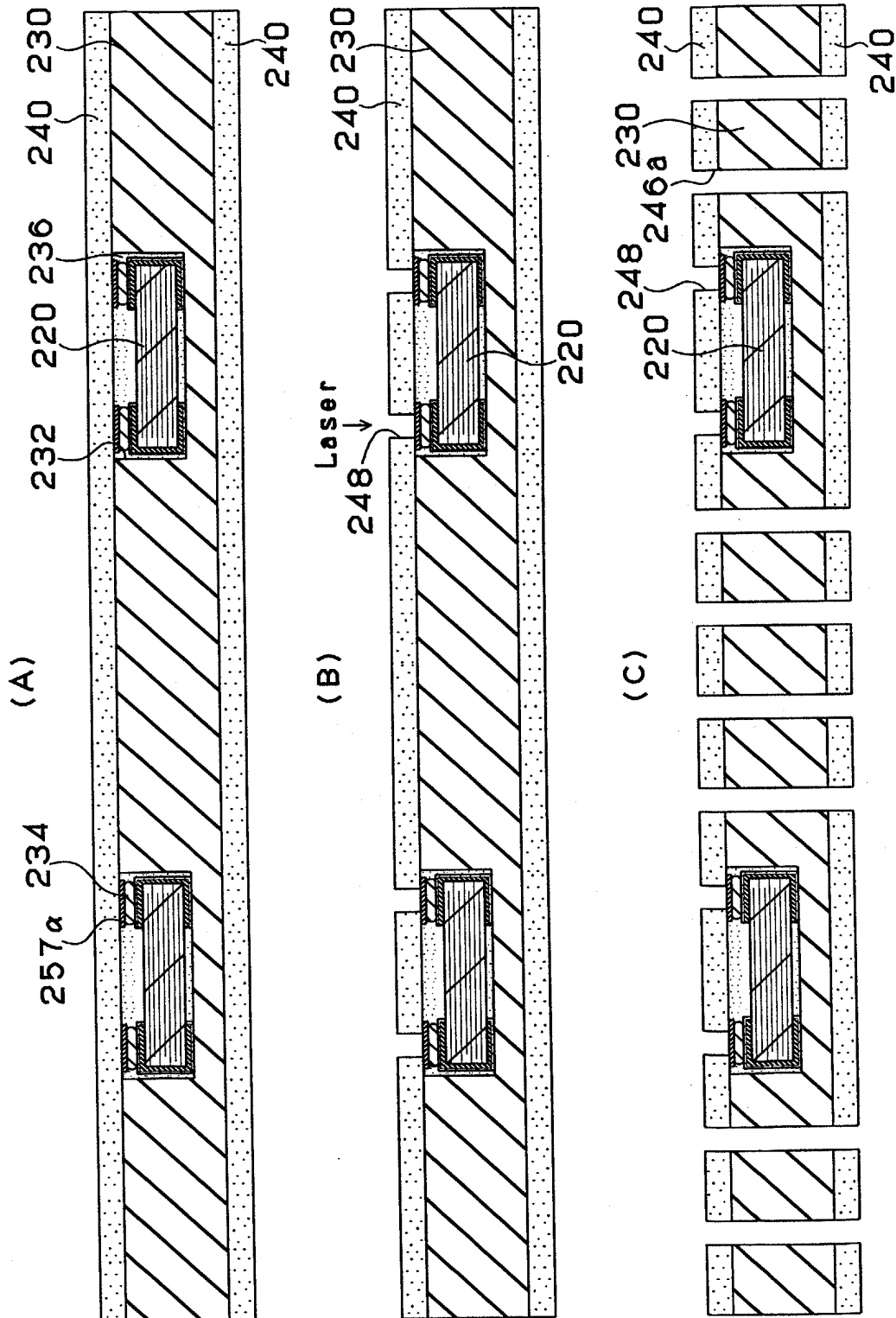


Fig. 24





25/73  
Fig. 25



26/73  
Fig. 26

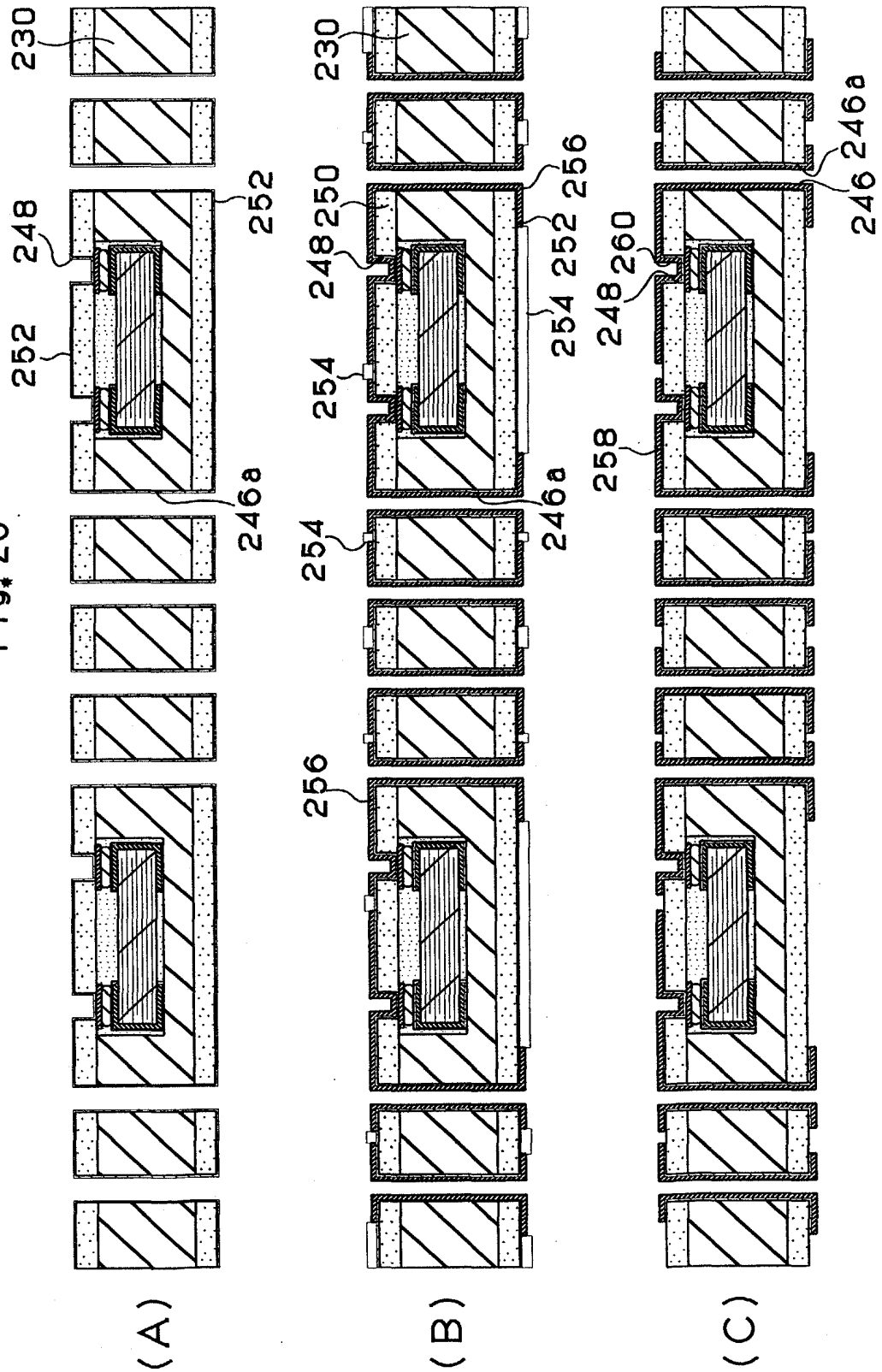
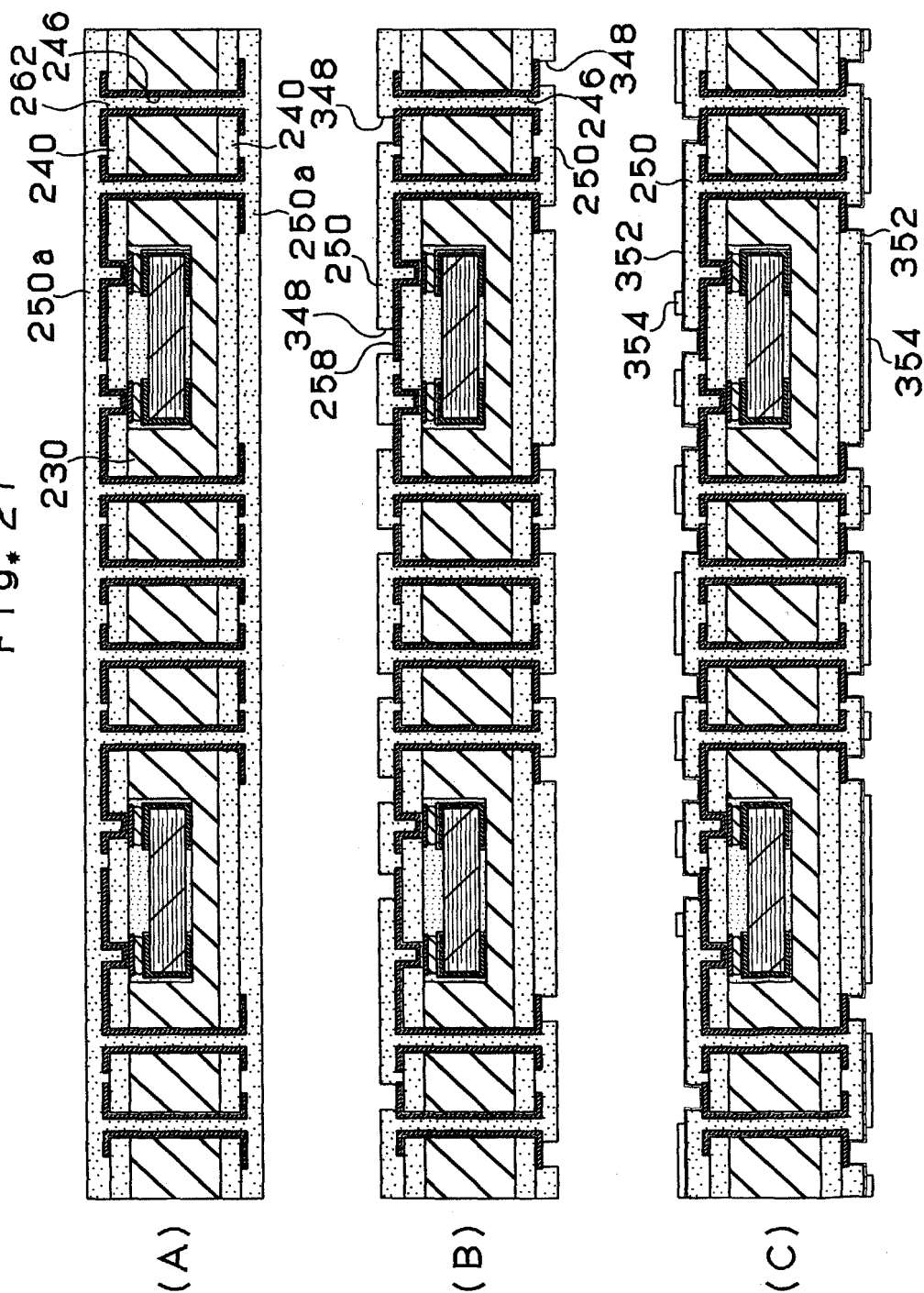
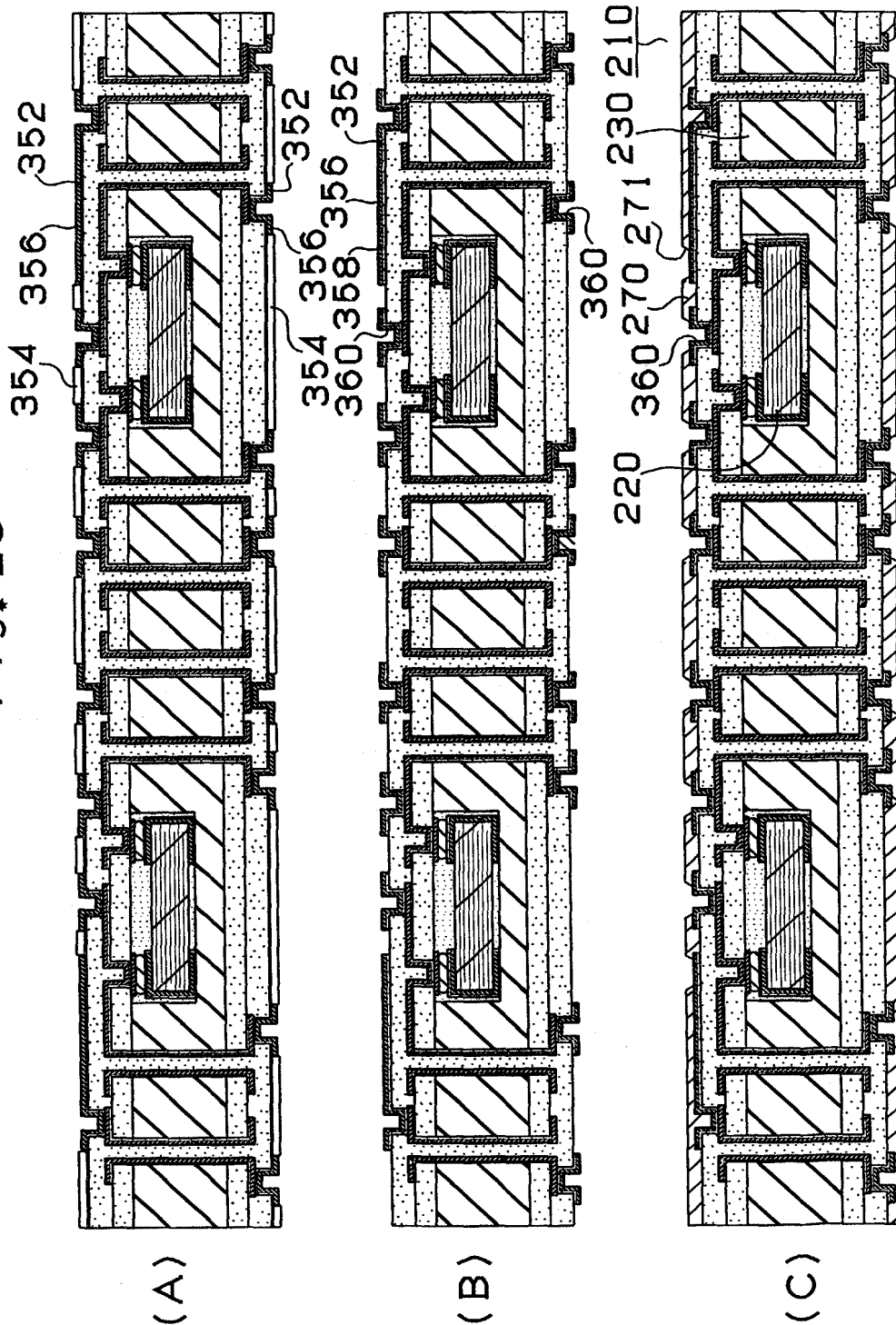


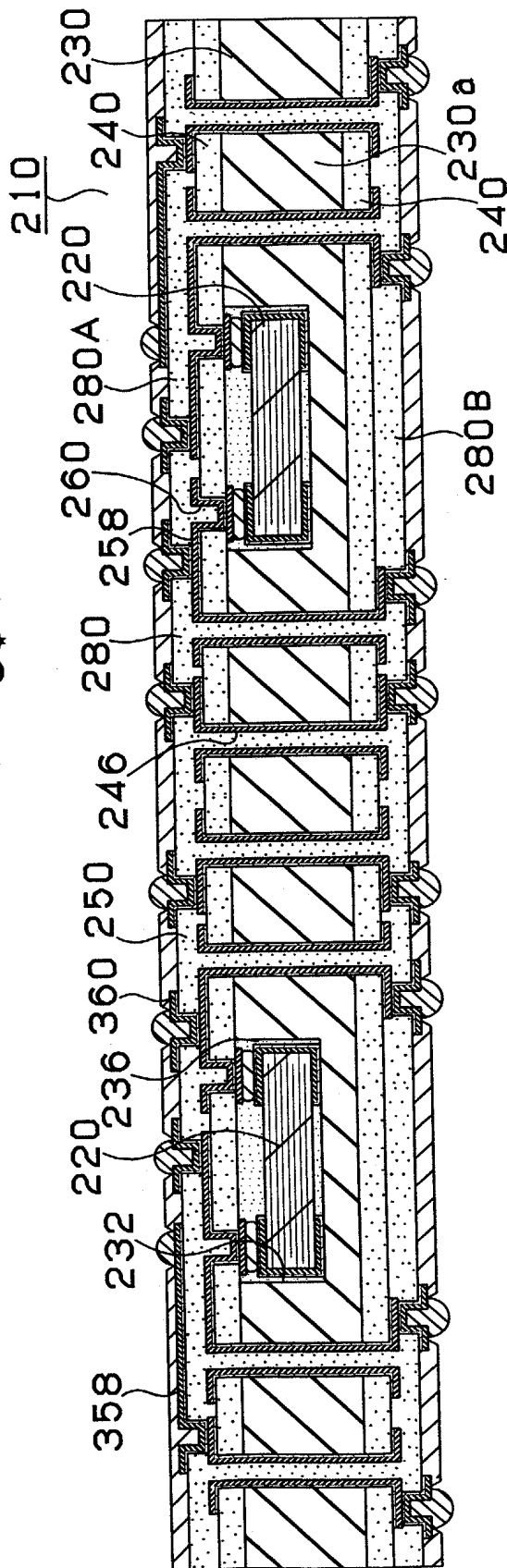
Fig. 27/73\*



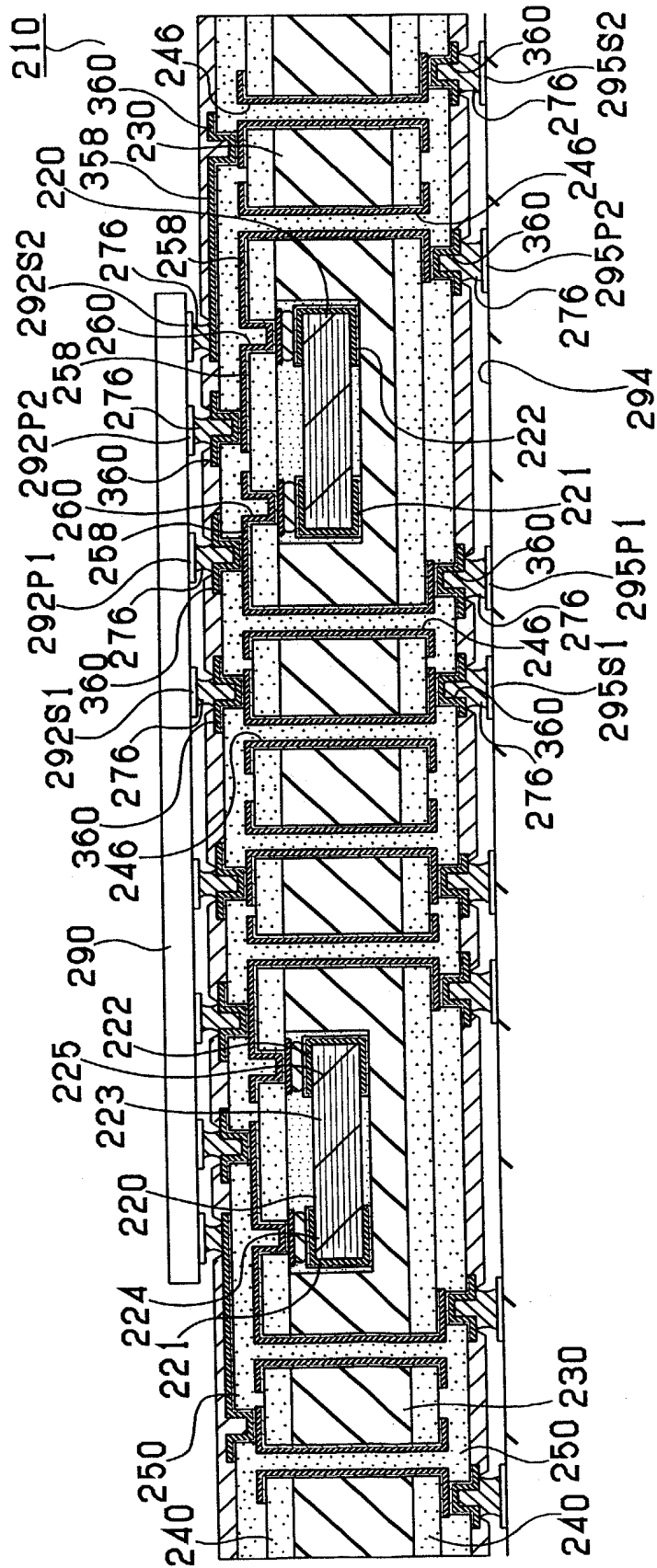
28/73  
Fig. 28



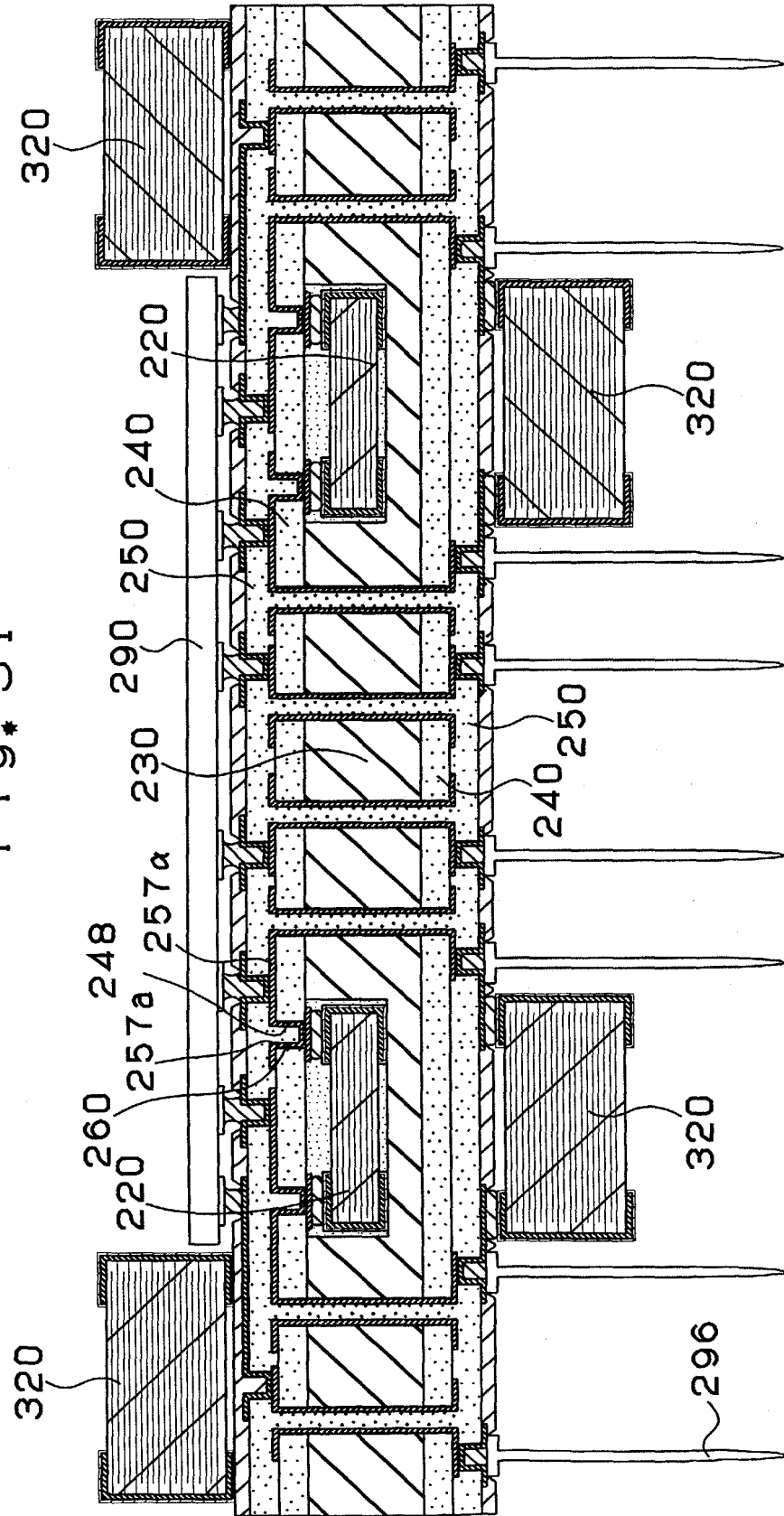
29/73  
Fig. 29



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31/73  
Fig. 31



32/73  
Fig. 32

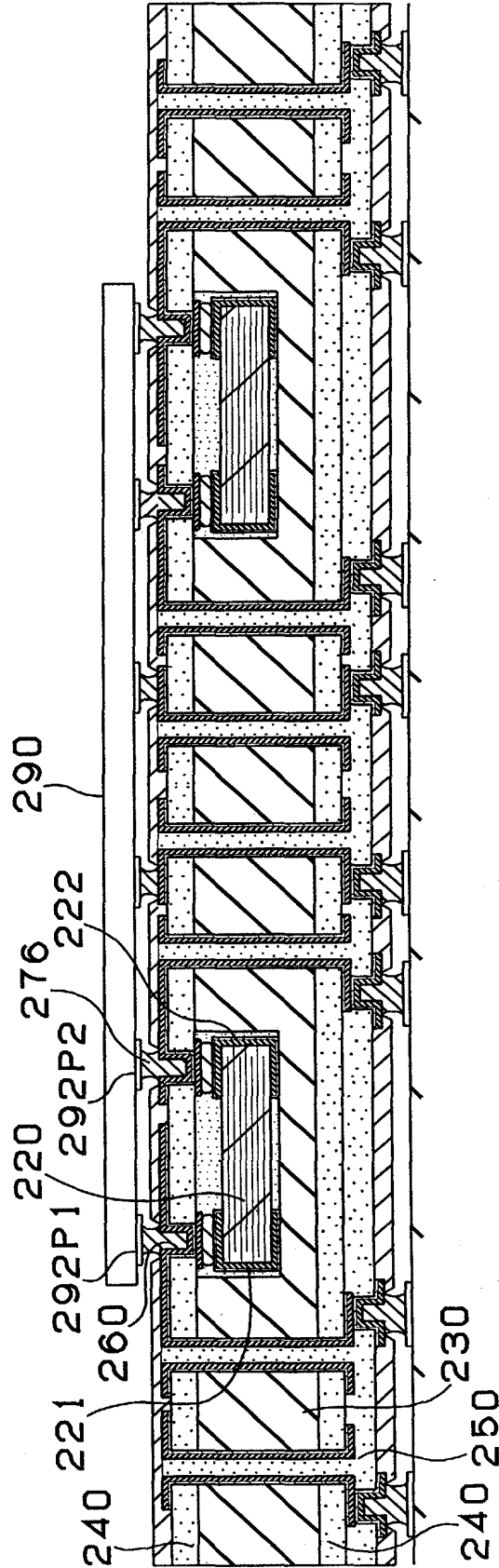




Fig. 33/73

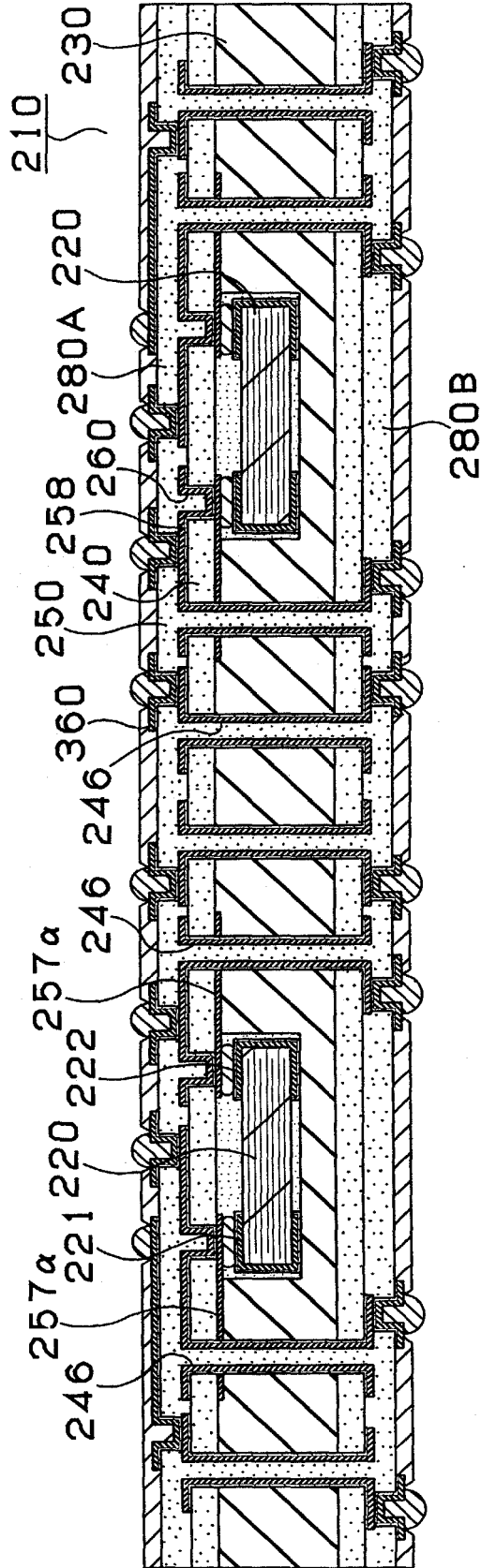
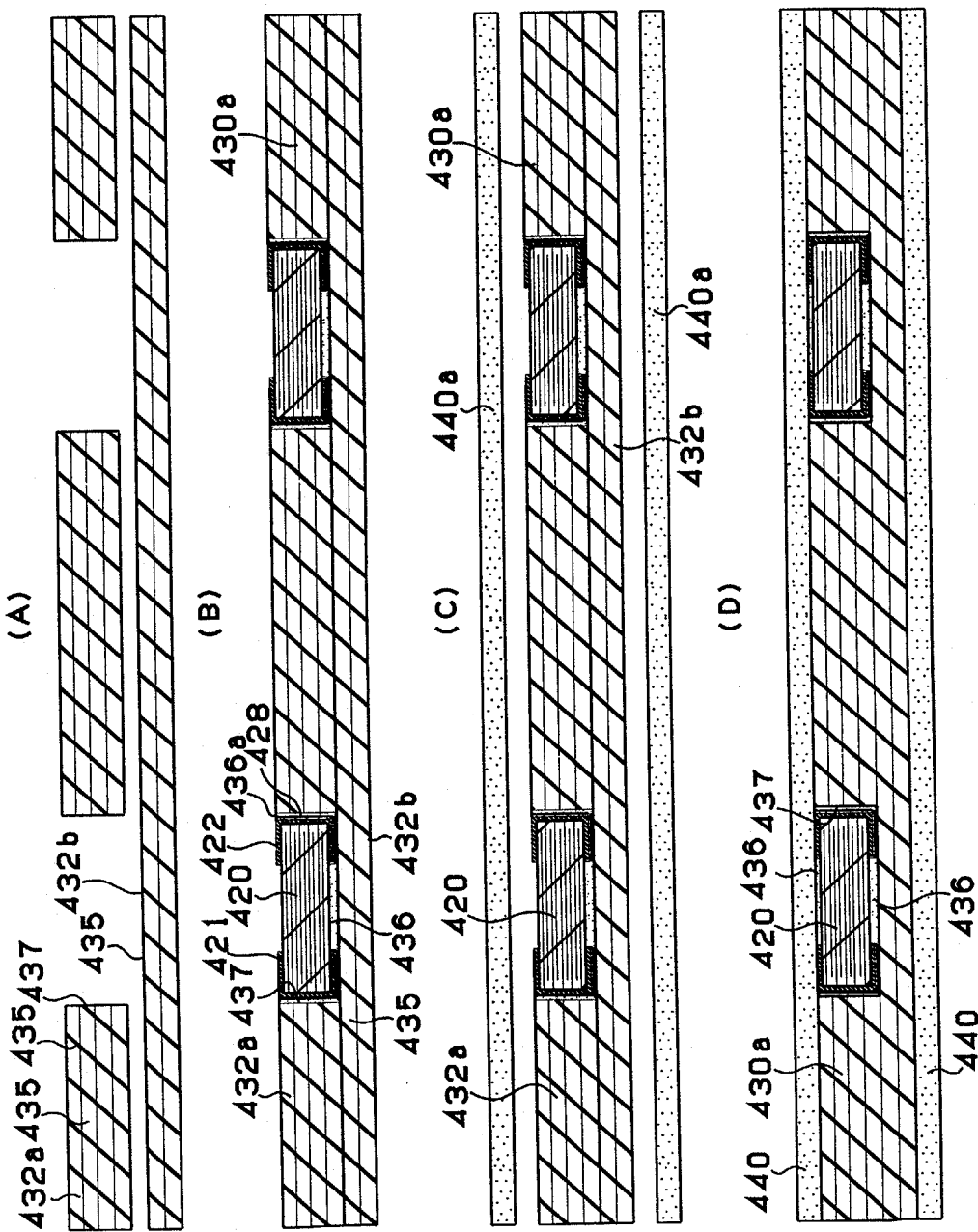
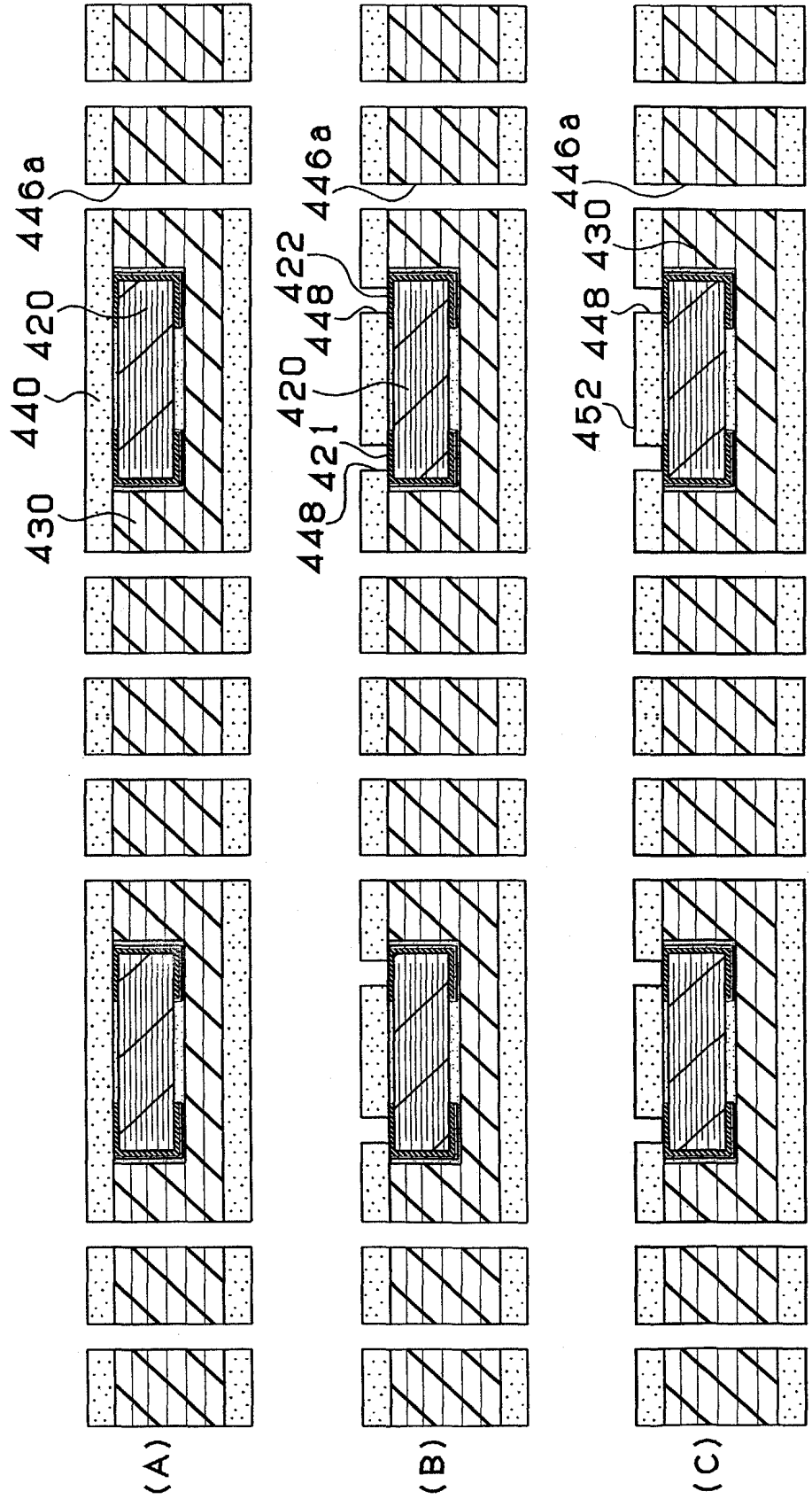
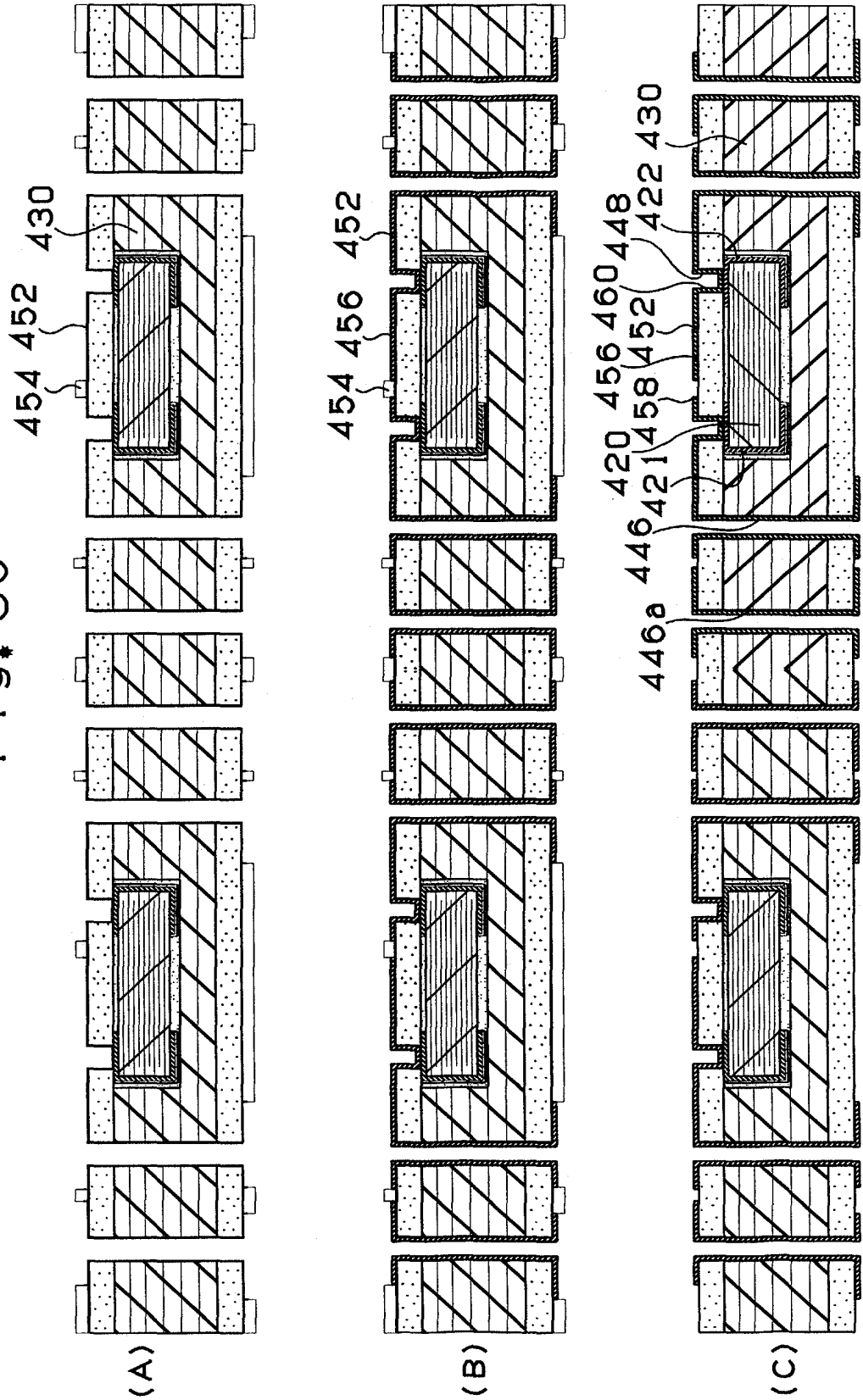


Fig. 34/734\*

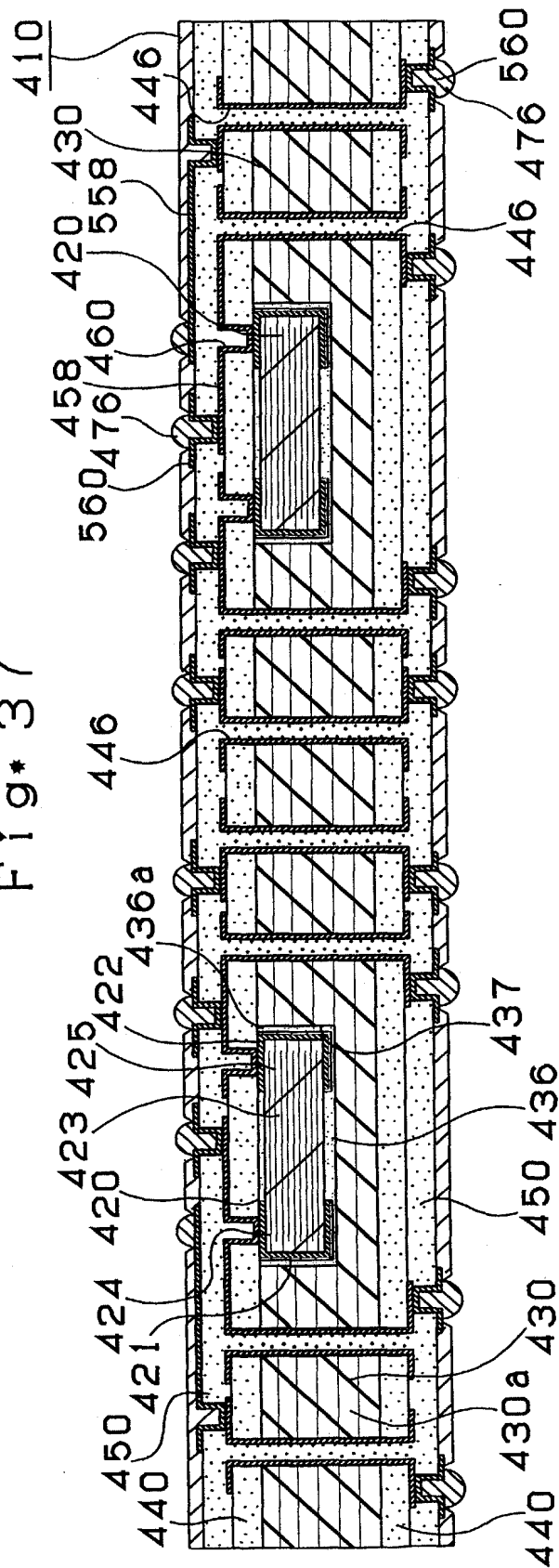




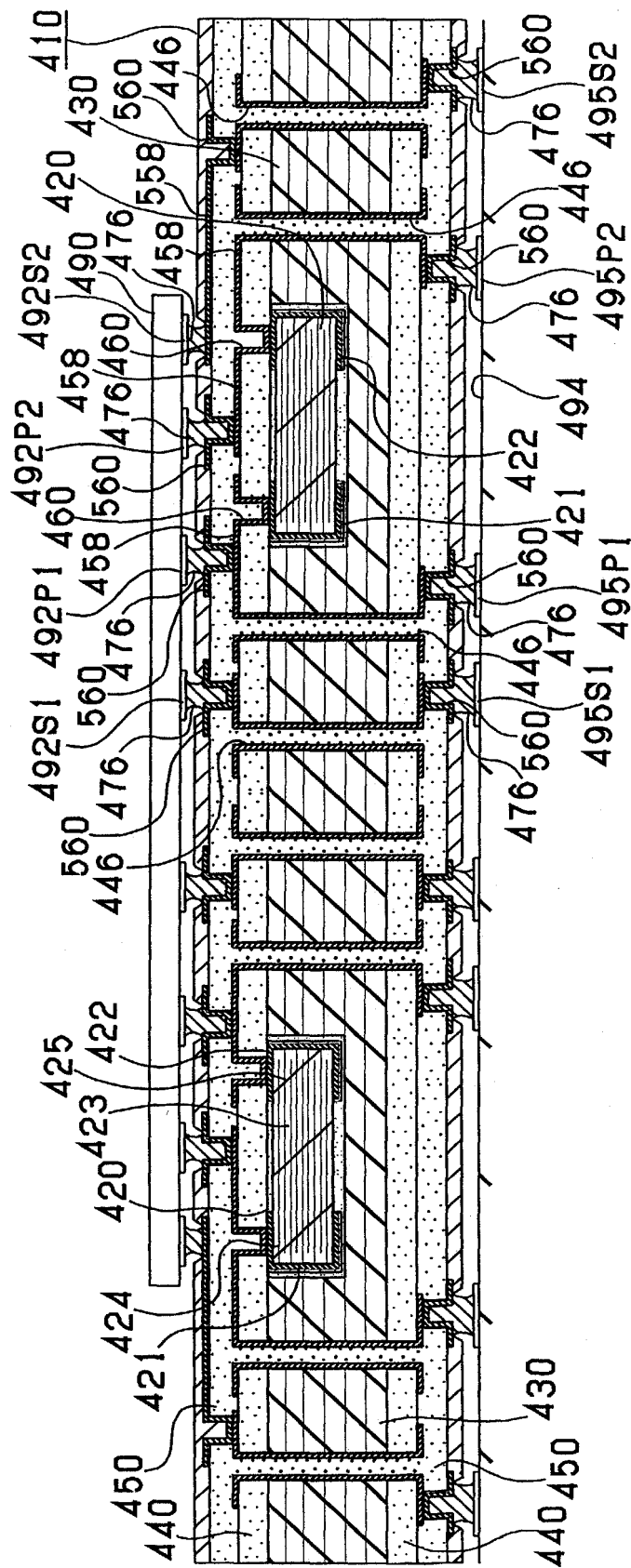
36/73  
Fig. 36



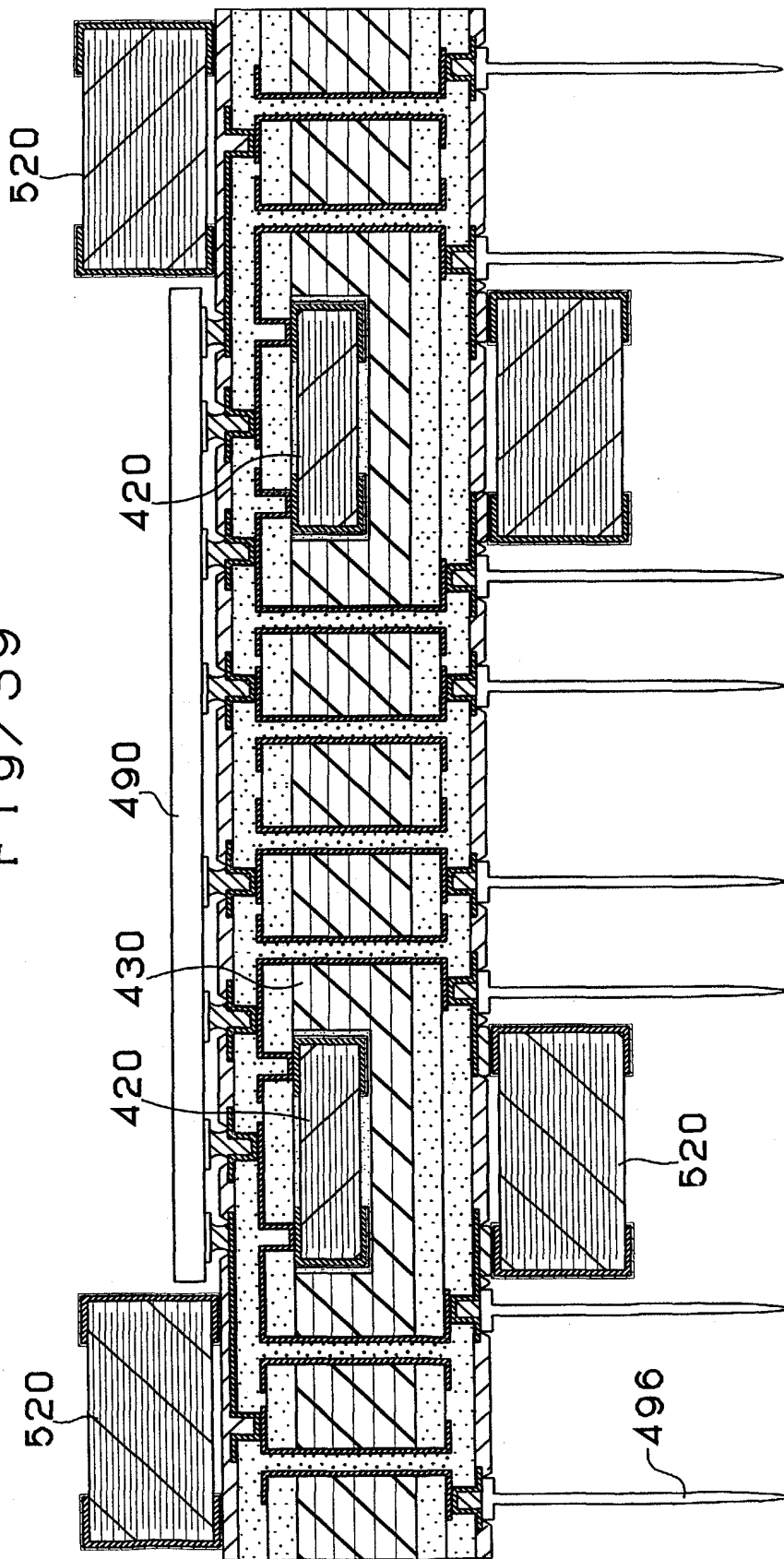
Fig\*37/37



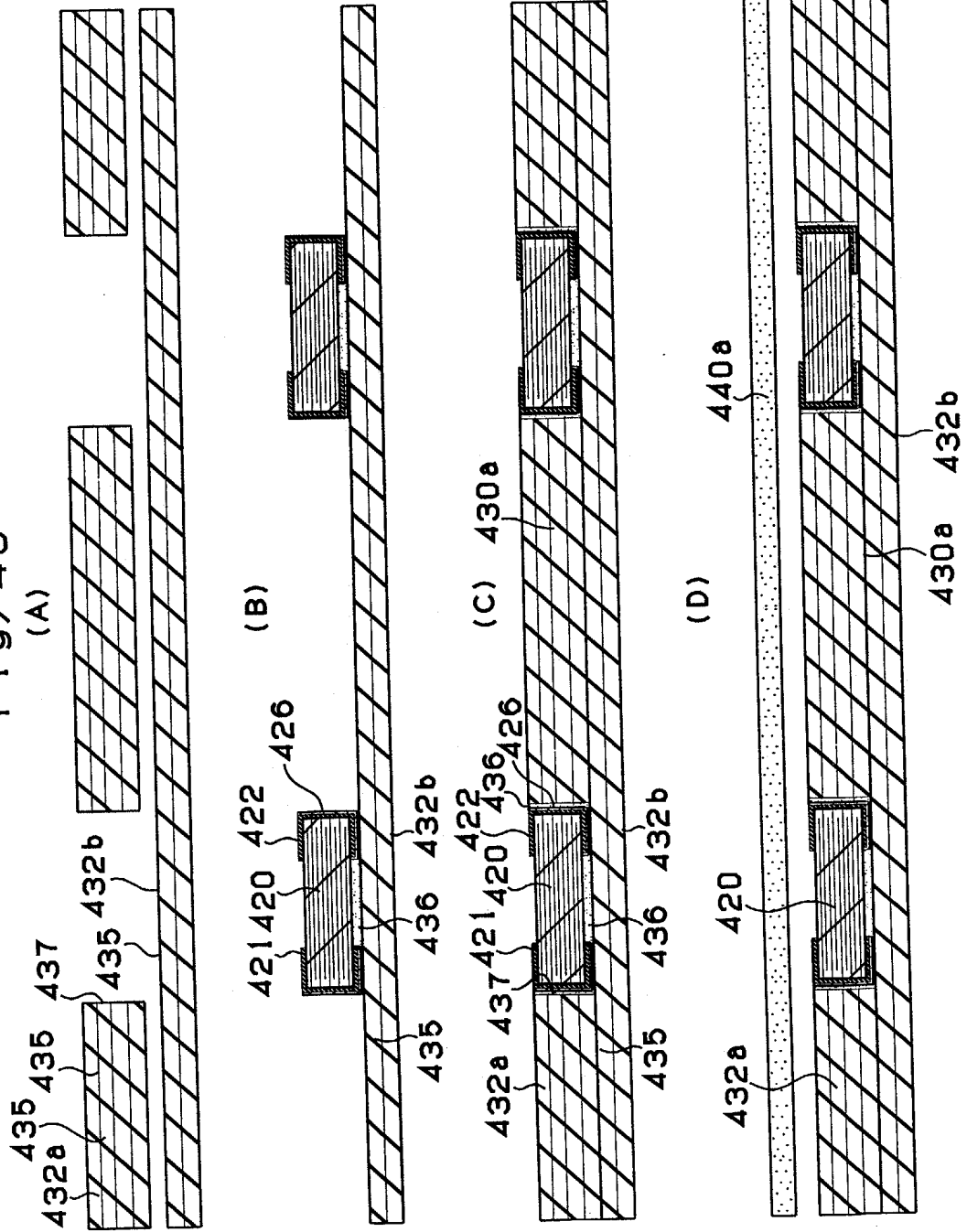
38/73  
Fig. 38



39/73  
Fig/39

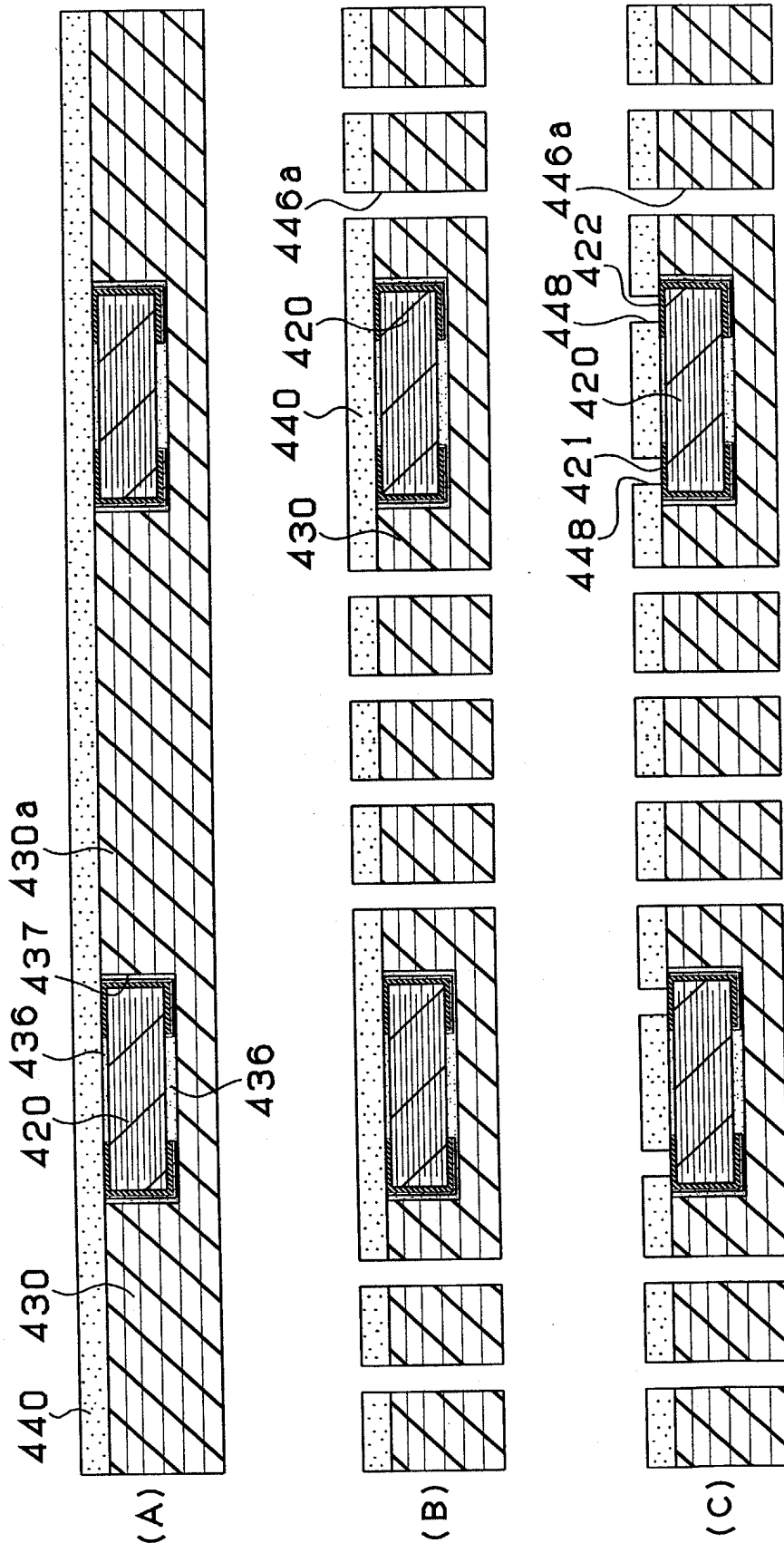


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Fig/40

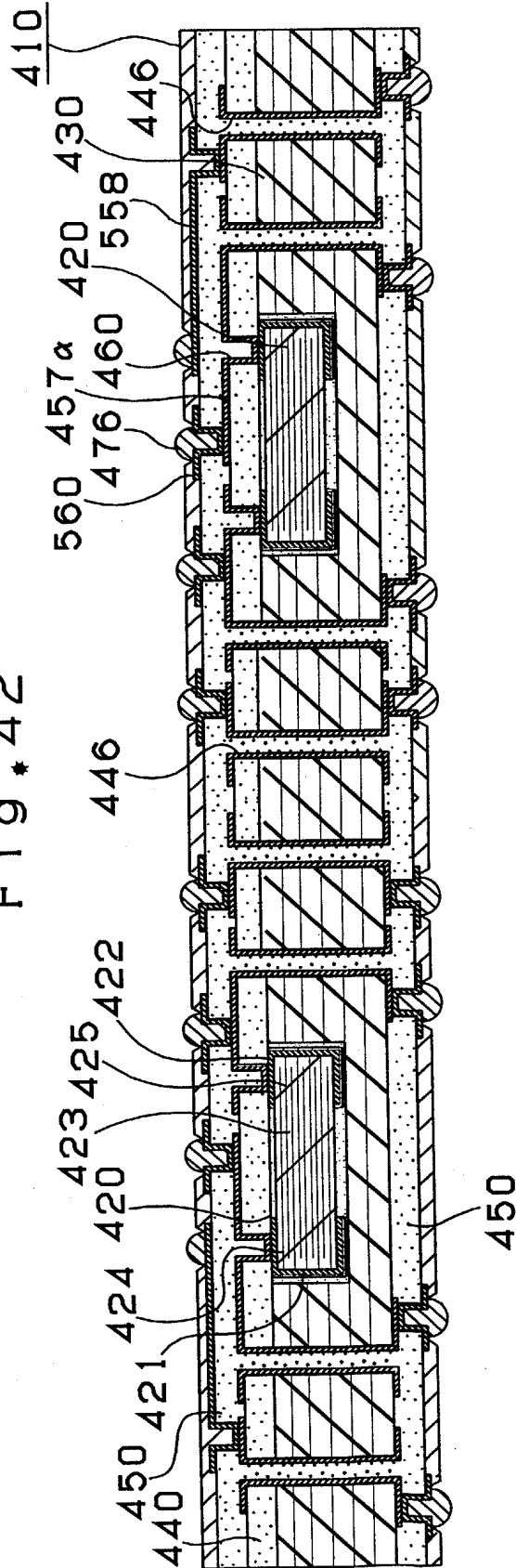




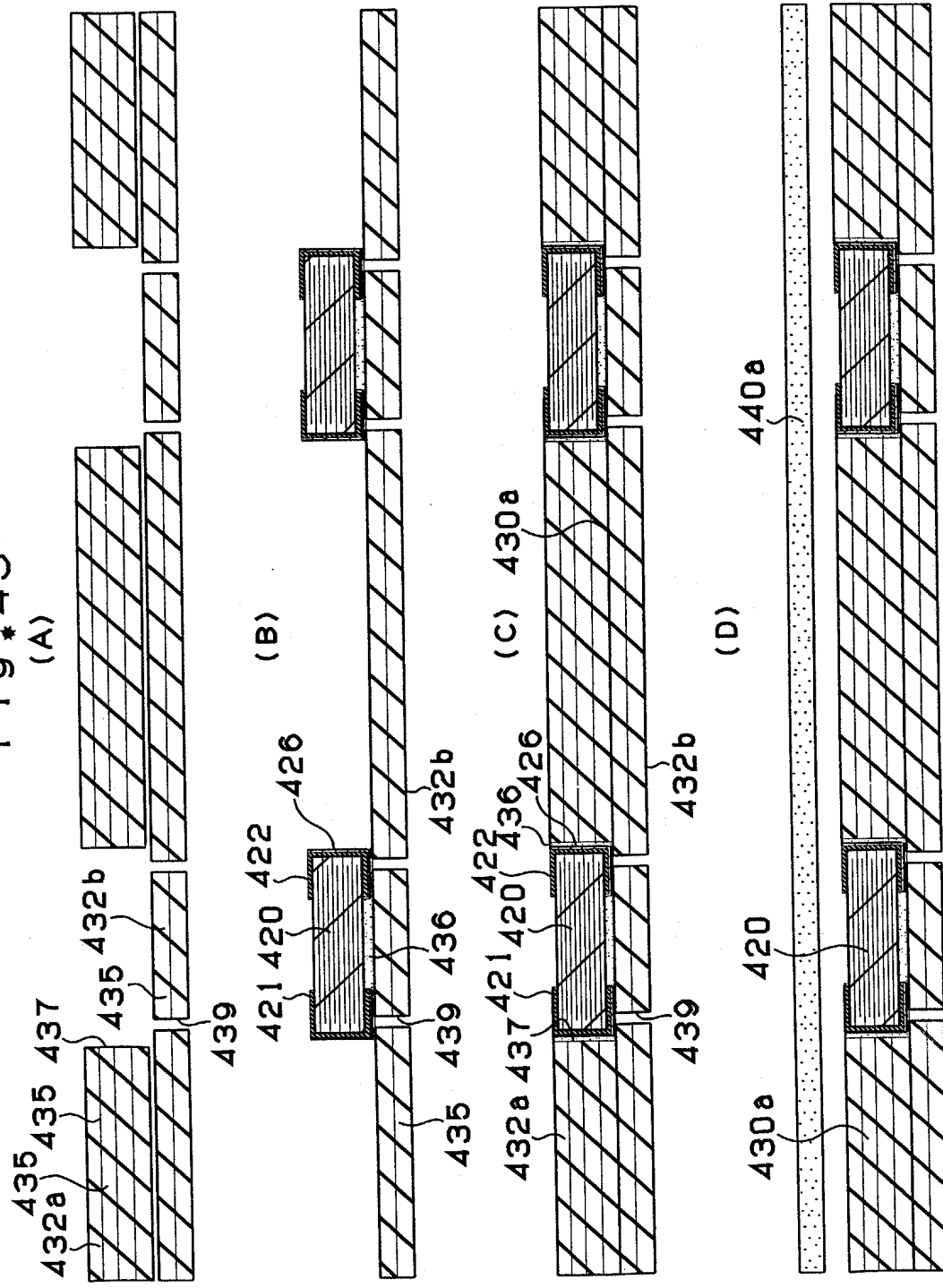
41/73  
Fig. 41



42/73  
Fig. 42



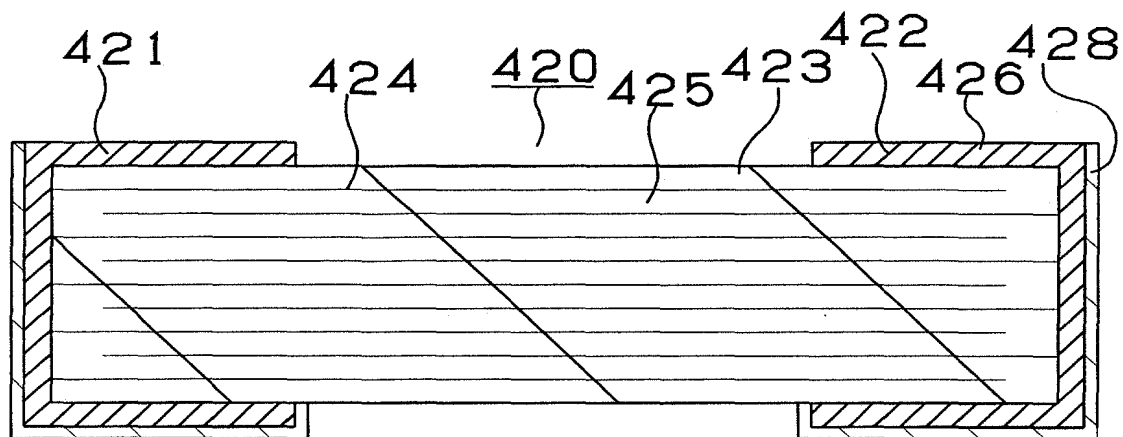
43/73  
Fig. 43



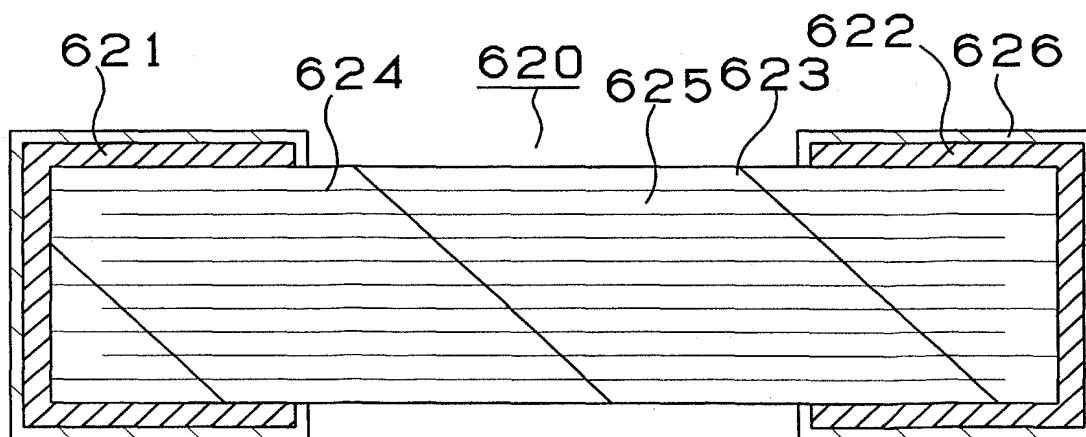


45/73  
Fig. 45

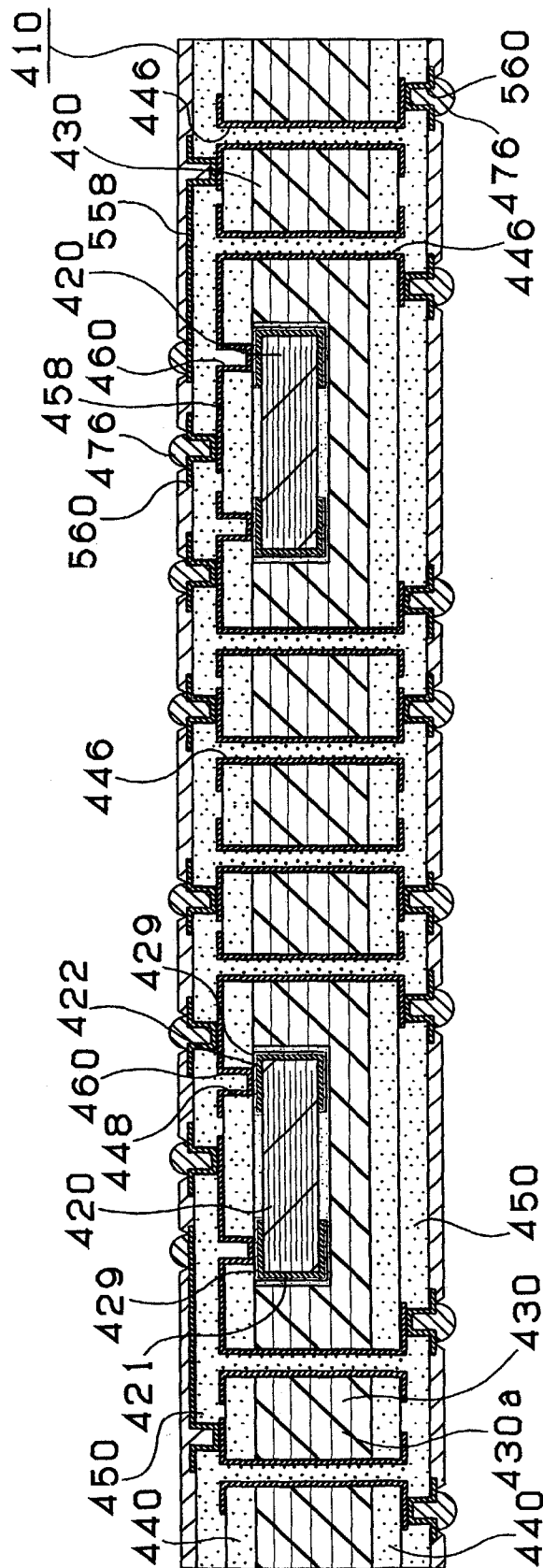
(A)



(B)



46/73  
Fig. 46



47/73  
Fig. 47

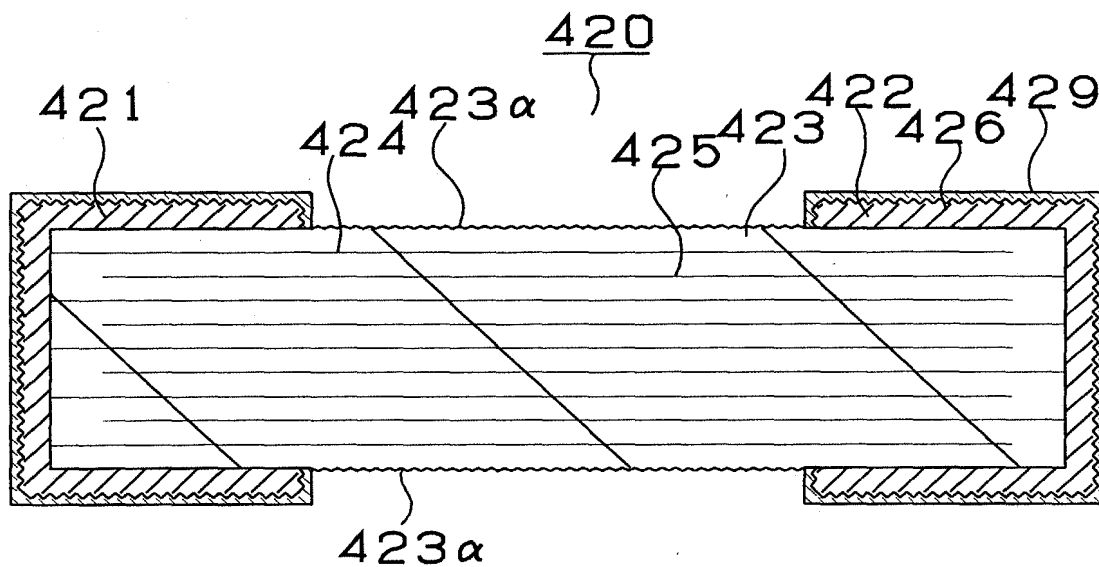
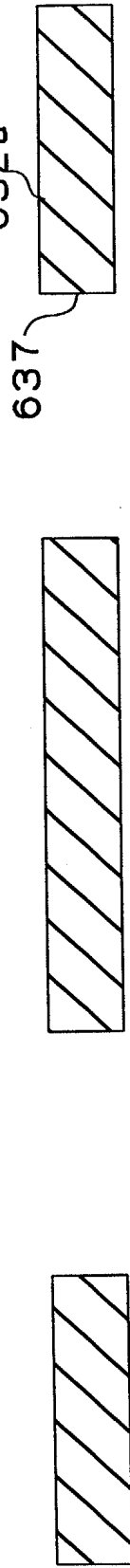


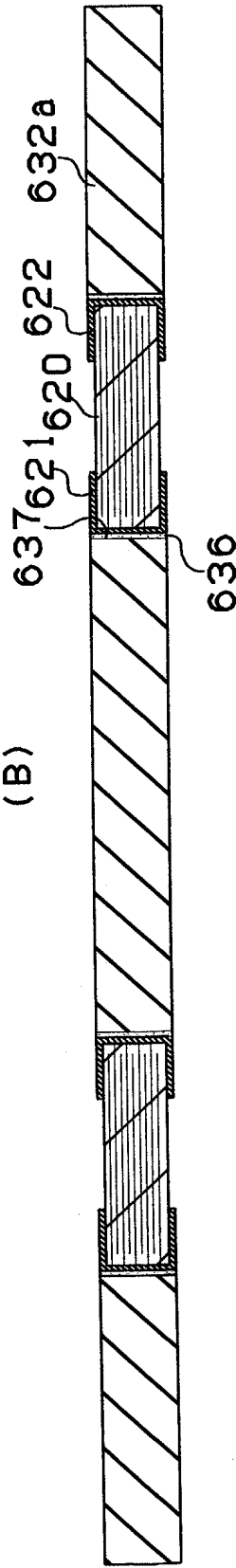
FIG. 47

48/73  
Fig. 48

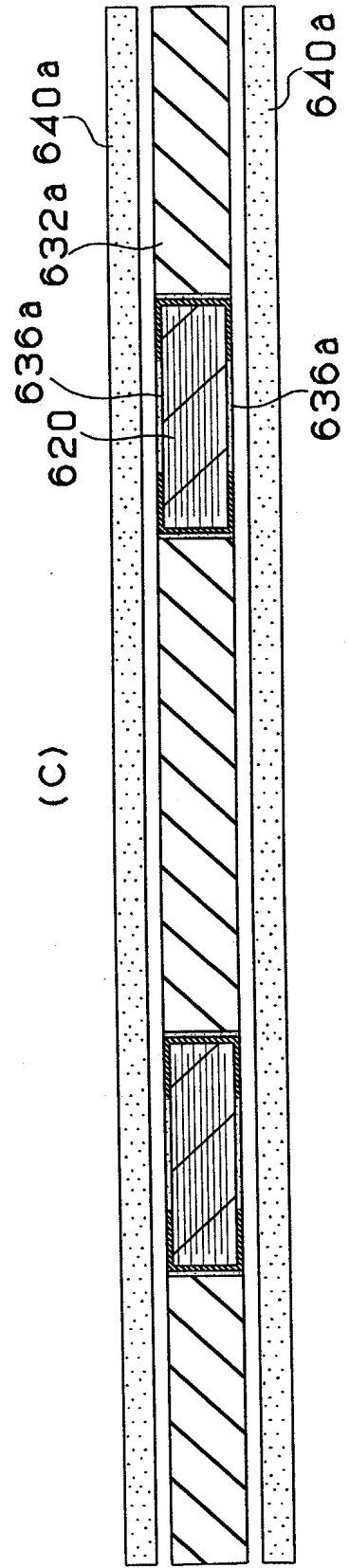
(A)



(B)

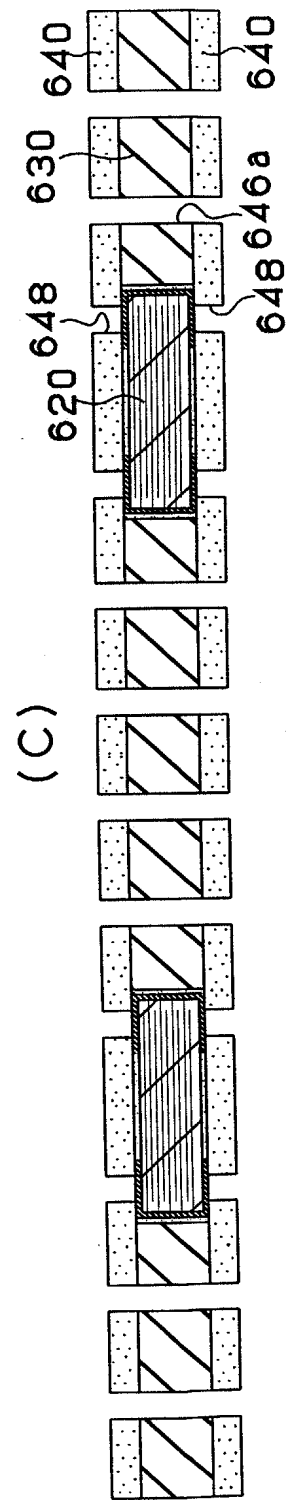
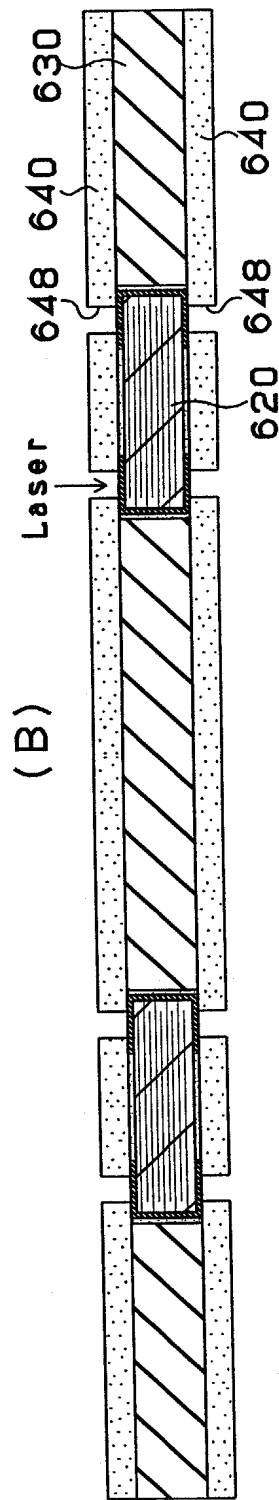
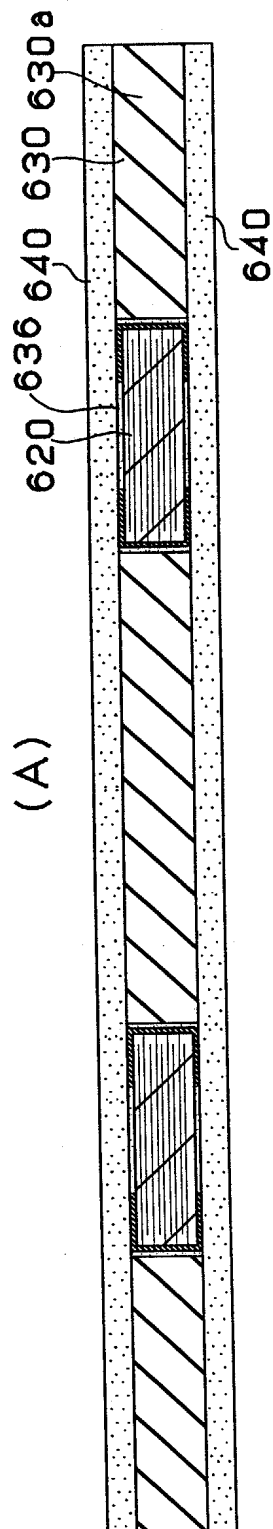


(C)





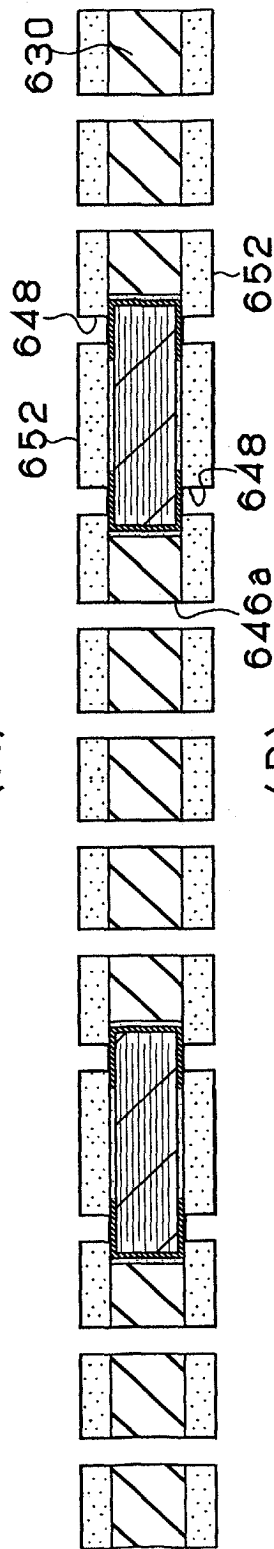
49/73  
Fig. 49



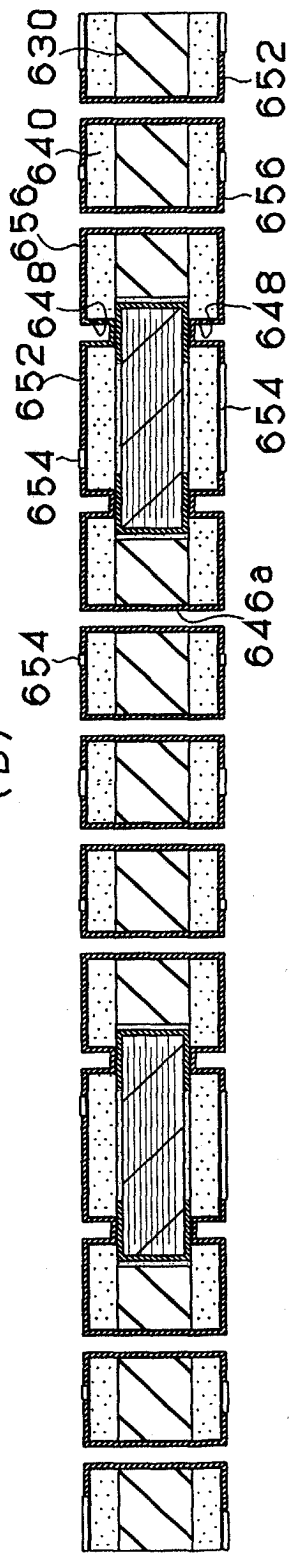
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50/73  
Fig. 50

(A)



(B)



(C)

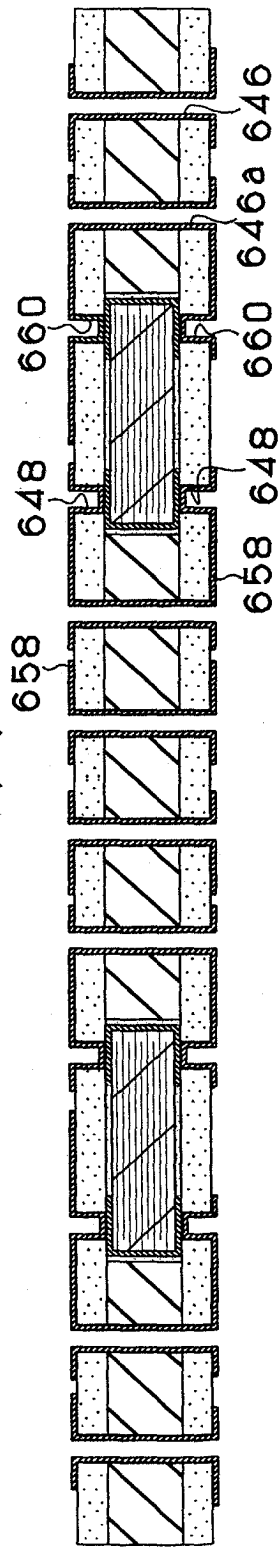
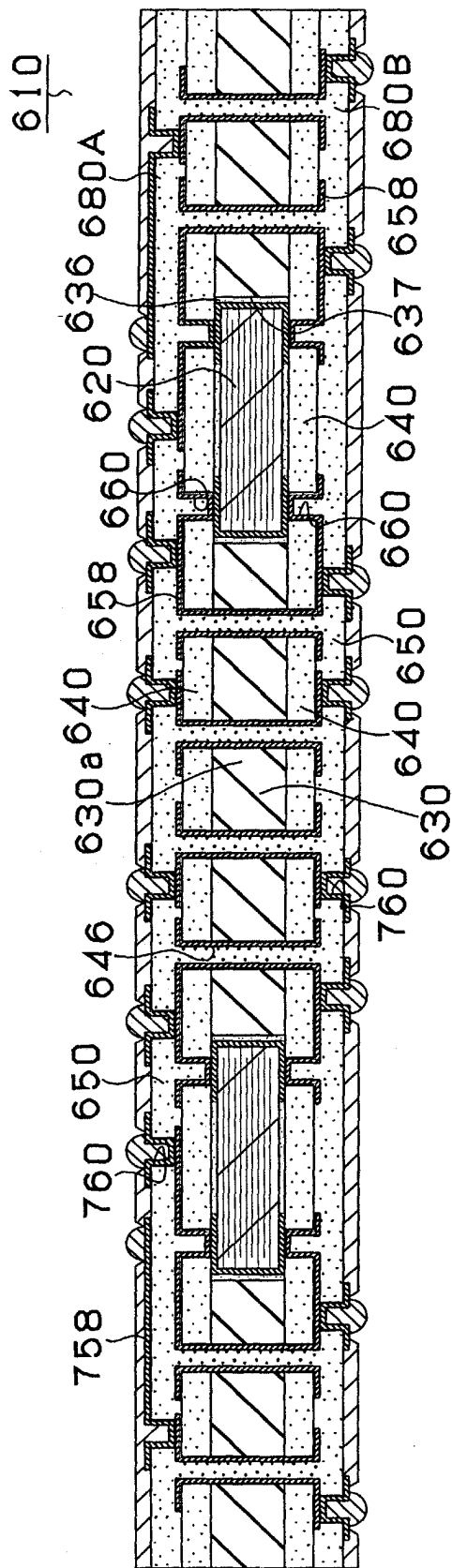
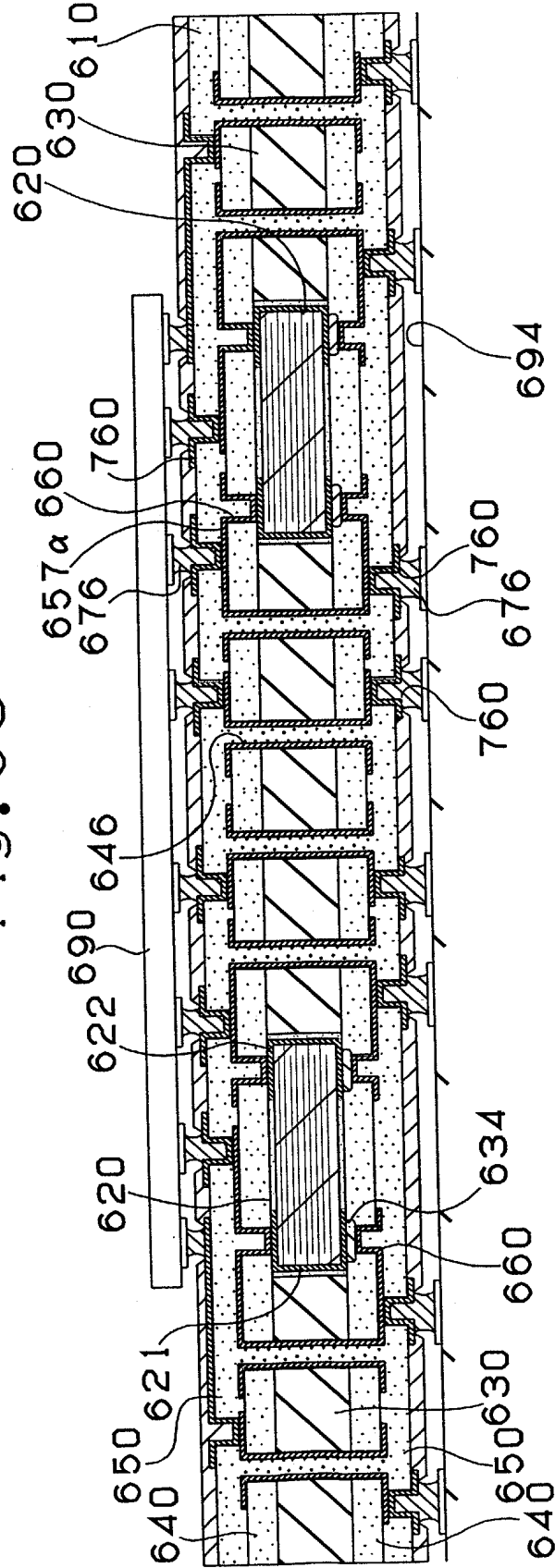


Fig. 51.51  
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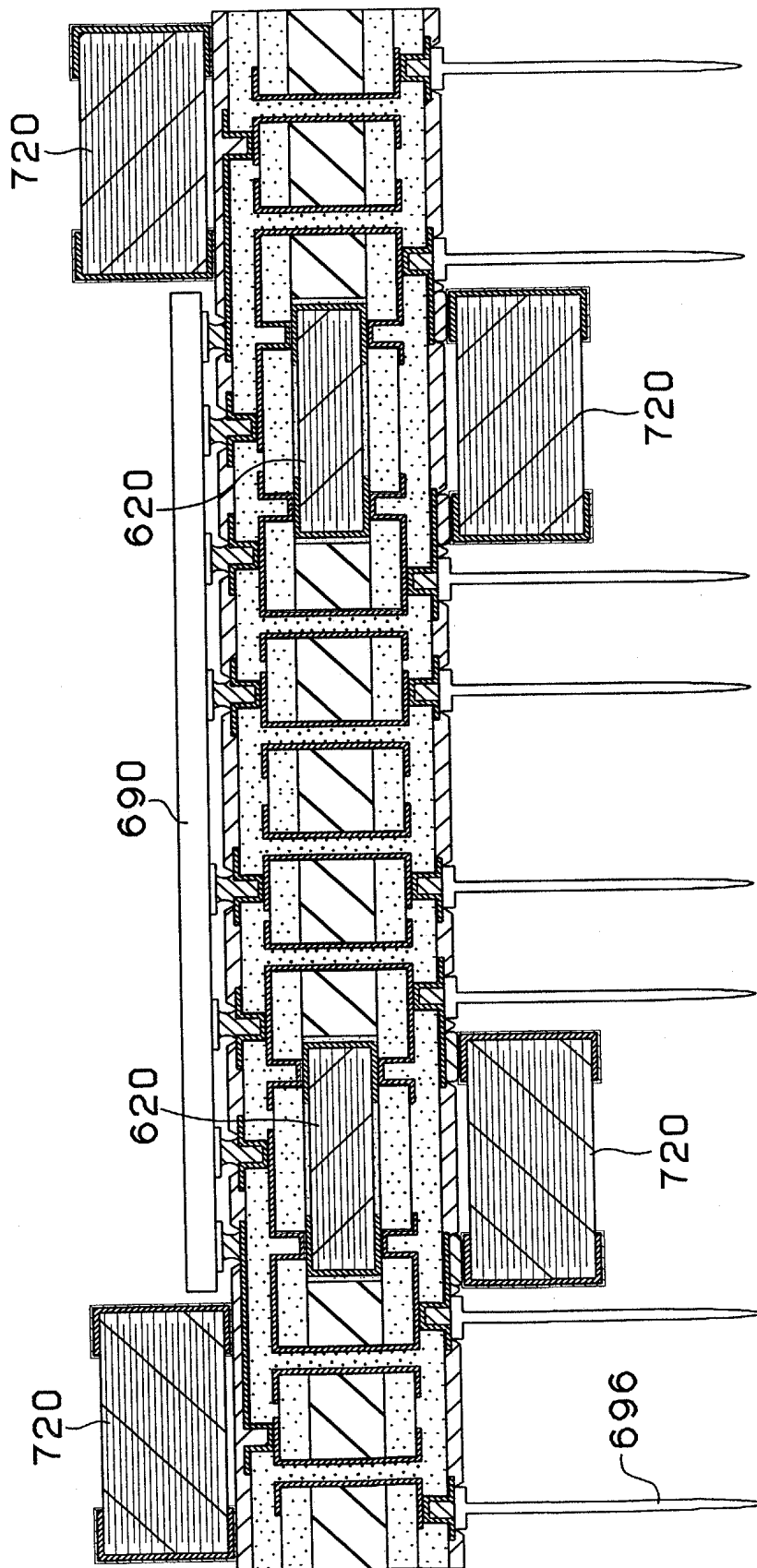


This diagram shows a cross-sectional view of a multi-layered semiconductor device. The structure consists of several layers and components, including a substrate (610) at the bottom, followed by a series of layers (620, 630, 640, 650, 660, 670, 680A, 680B, 690, 695S1, 695P1, 695S2, 695P2) and a top layer (610). The device features a central region (621) and a series of rectangular openings (622, 623, 624) in the top layer. The layers are separated by various materials, including a dielectric layer (640) and a conductive layer (650). The device is shown in a cross-sectional view, with the layers and components labeled with reference numerals.

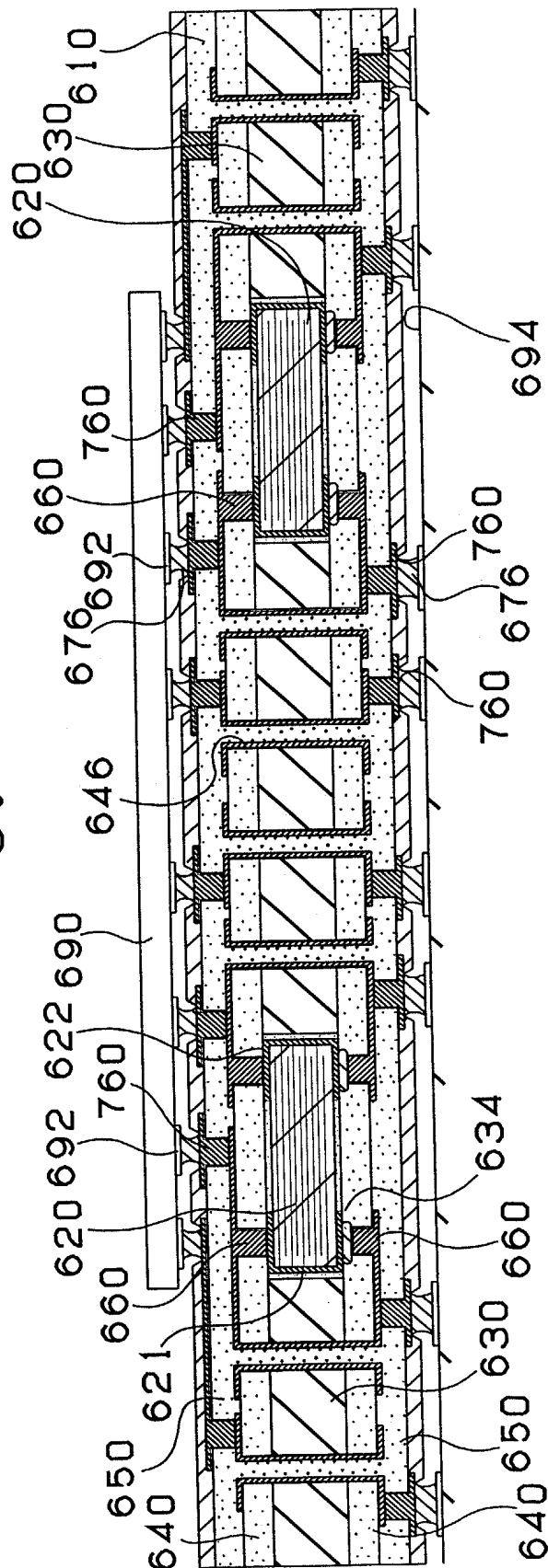
53/73  
Fig. 53



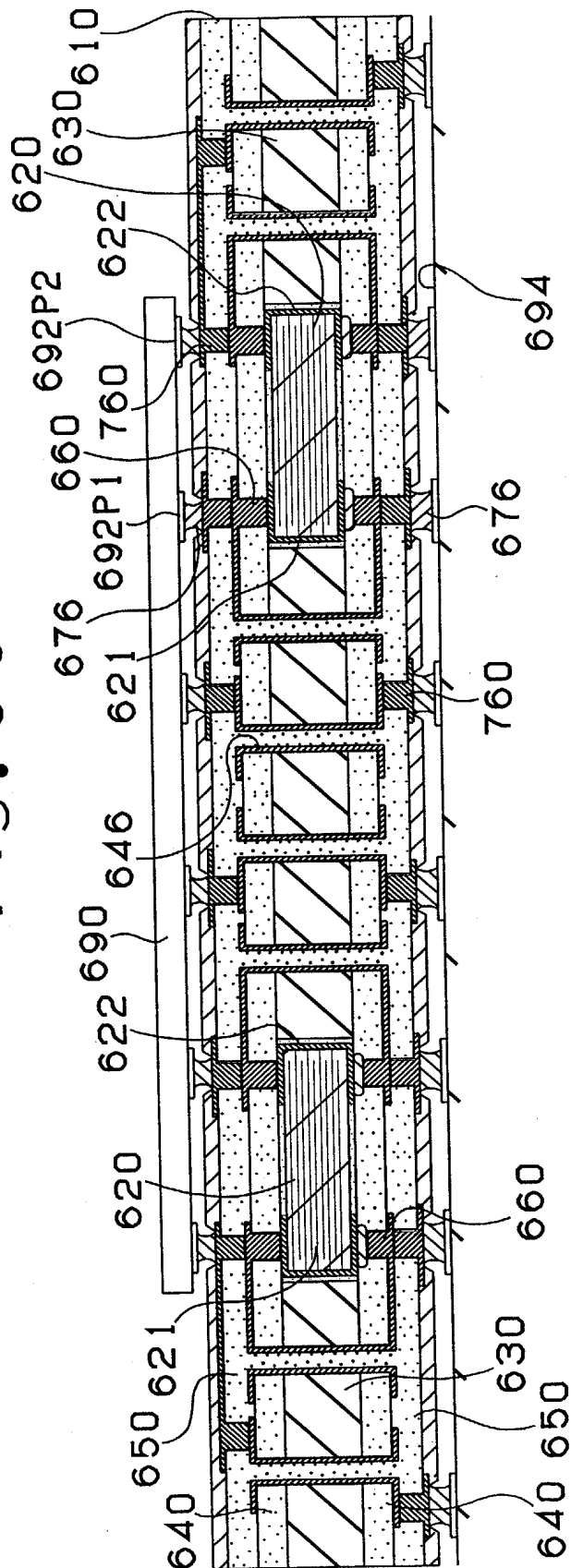
54/73  
Fig. 54



55/73  
Fig. 55

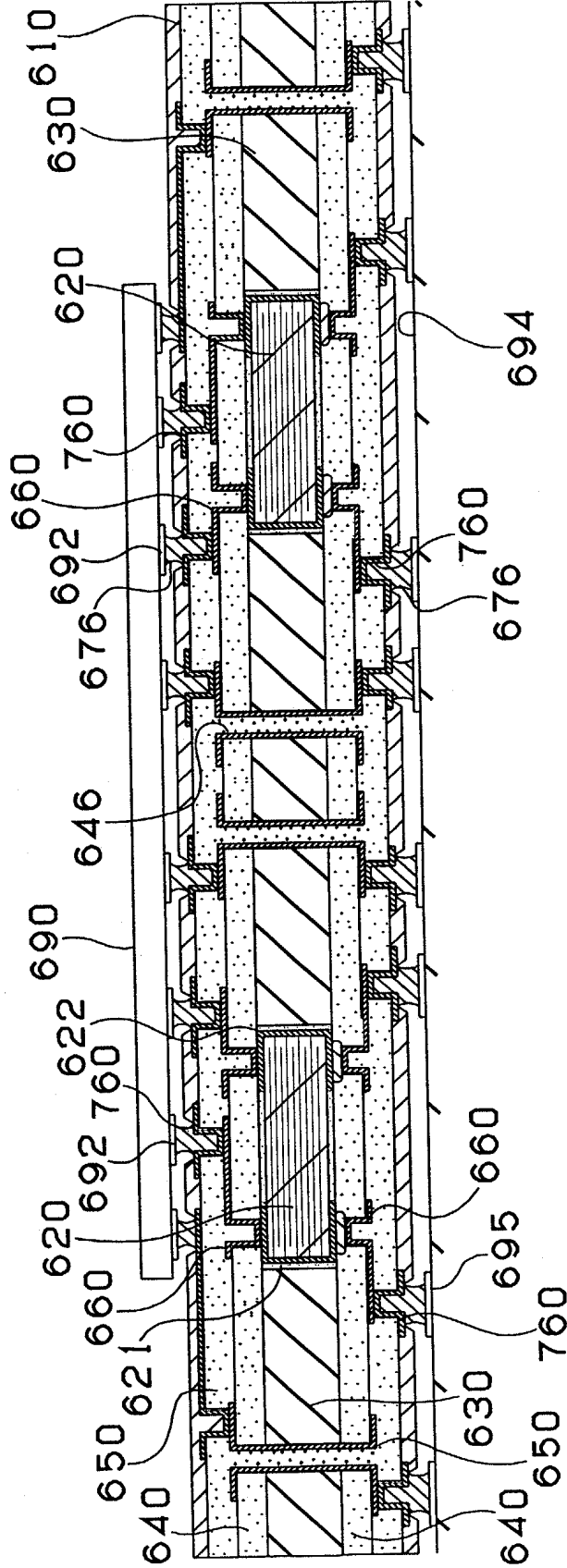


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Fig. 56

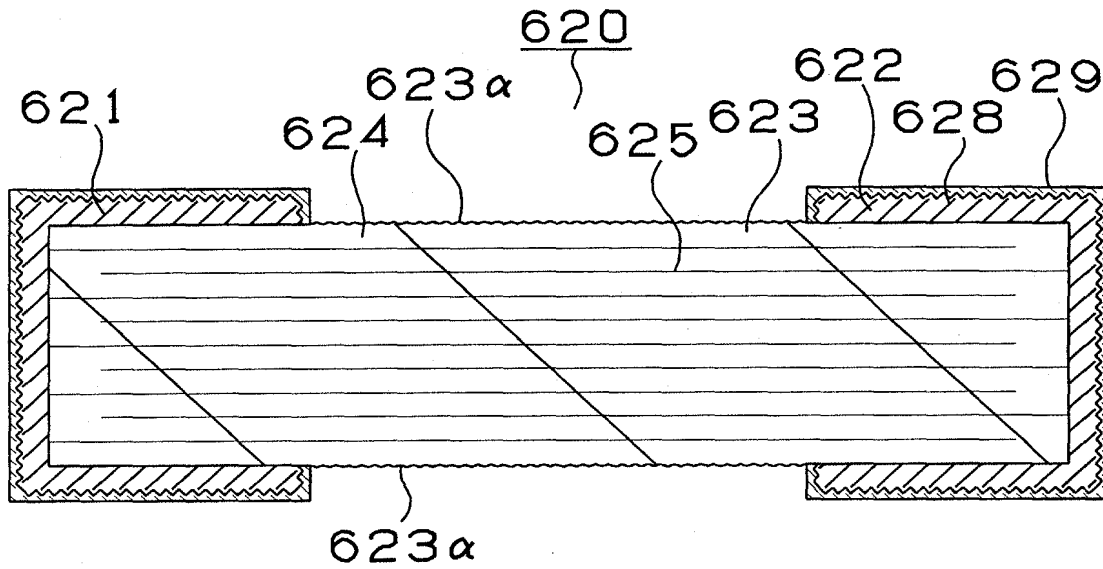




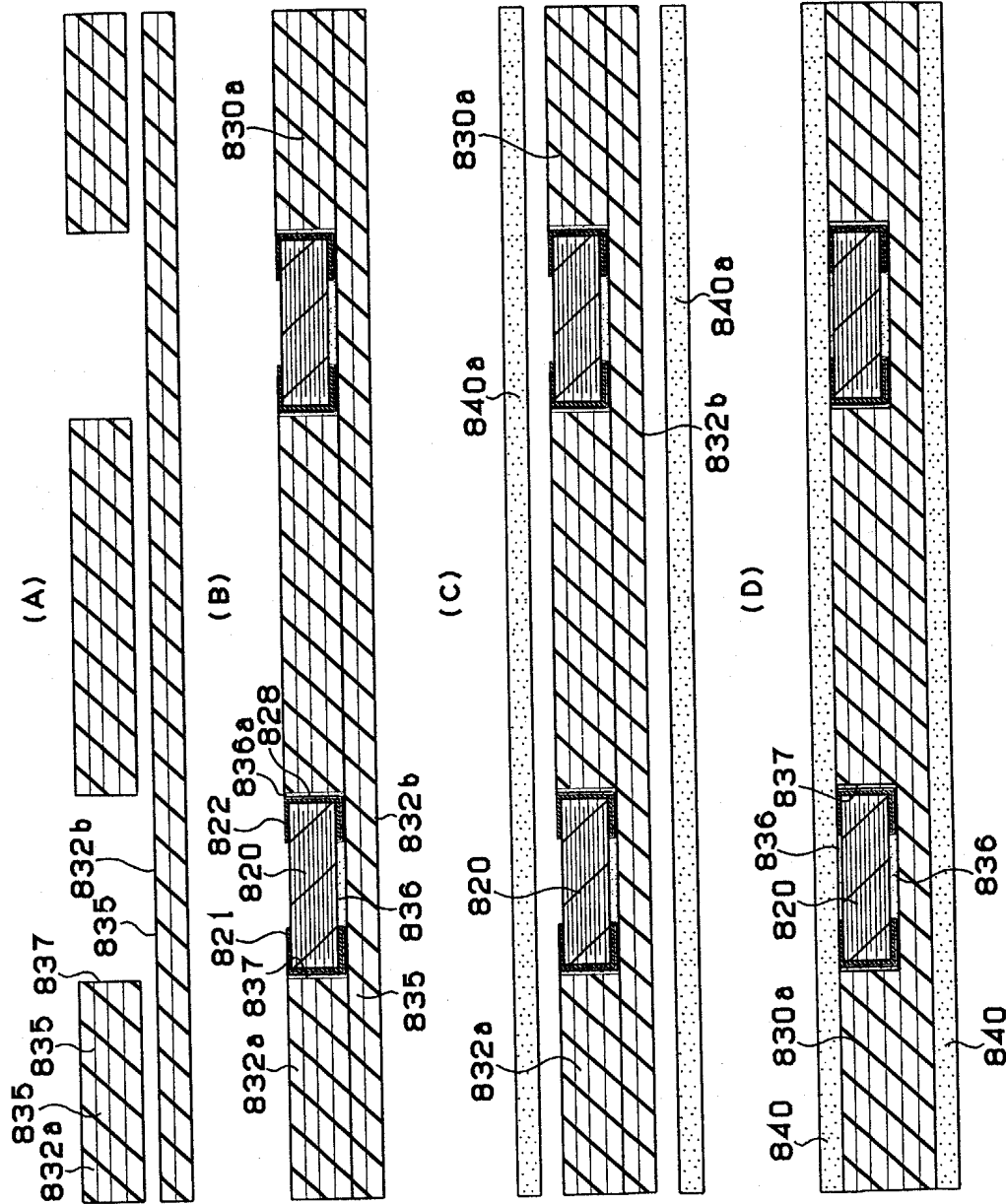
57/73  
Fig. 57



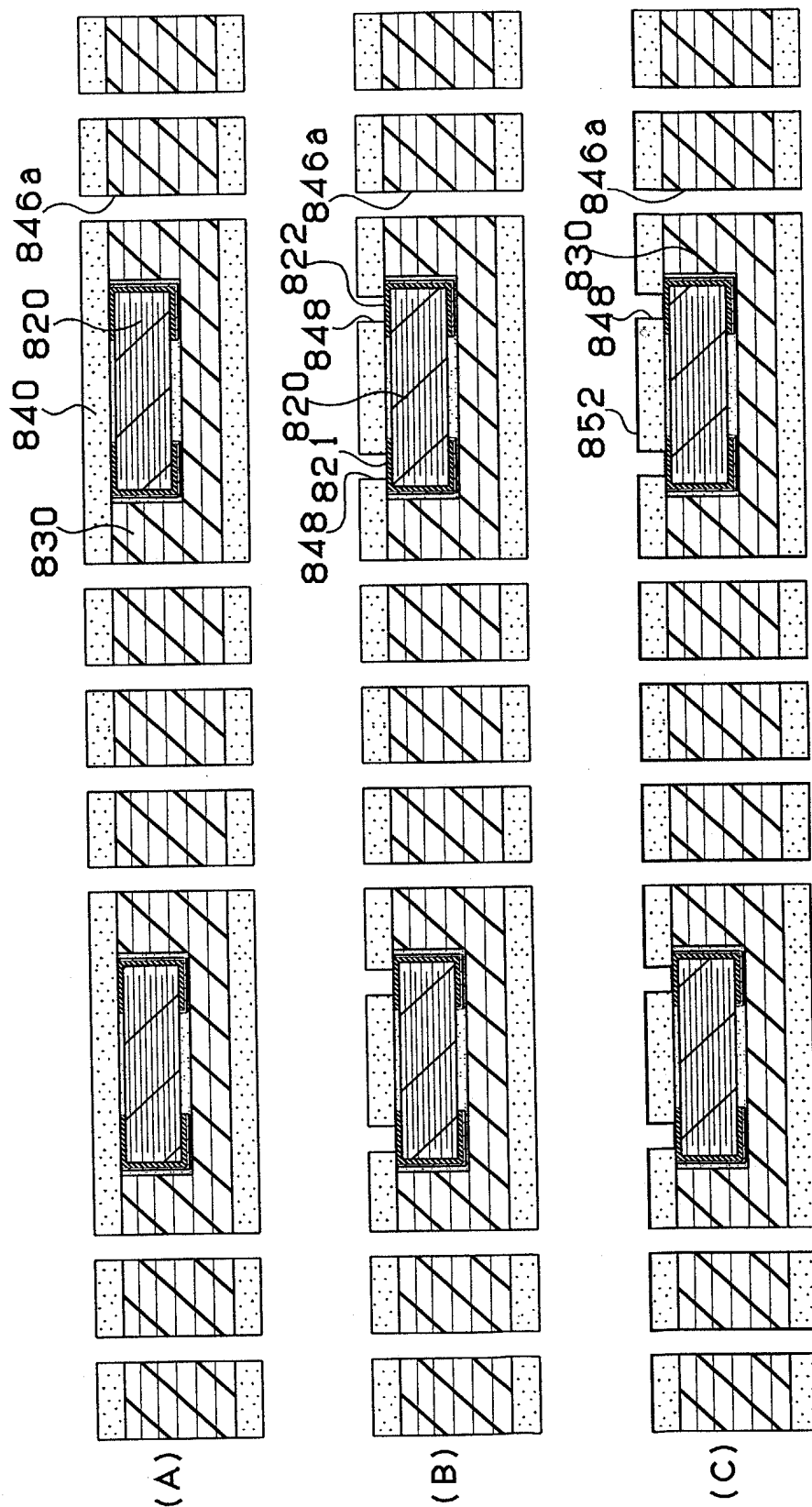


59/73  
Fig. 59

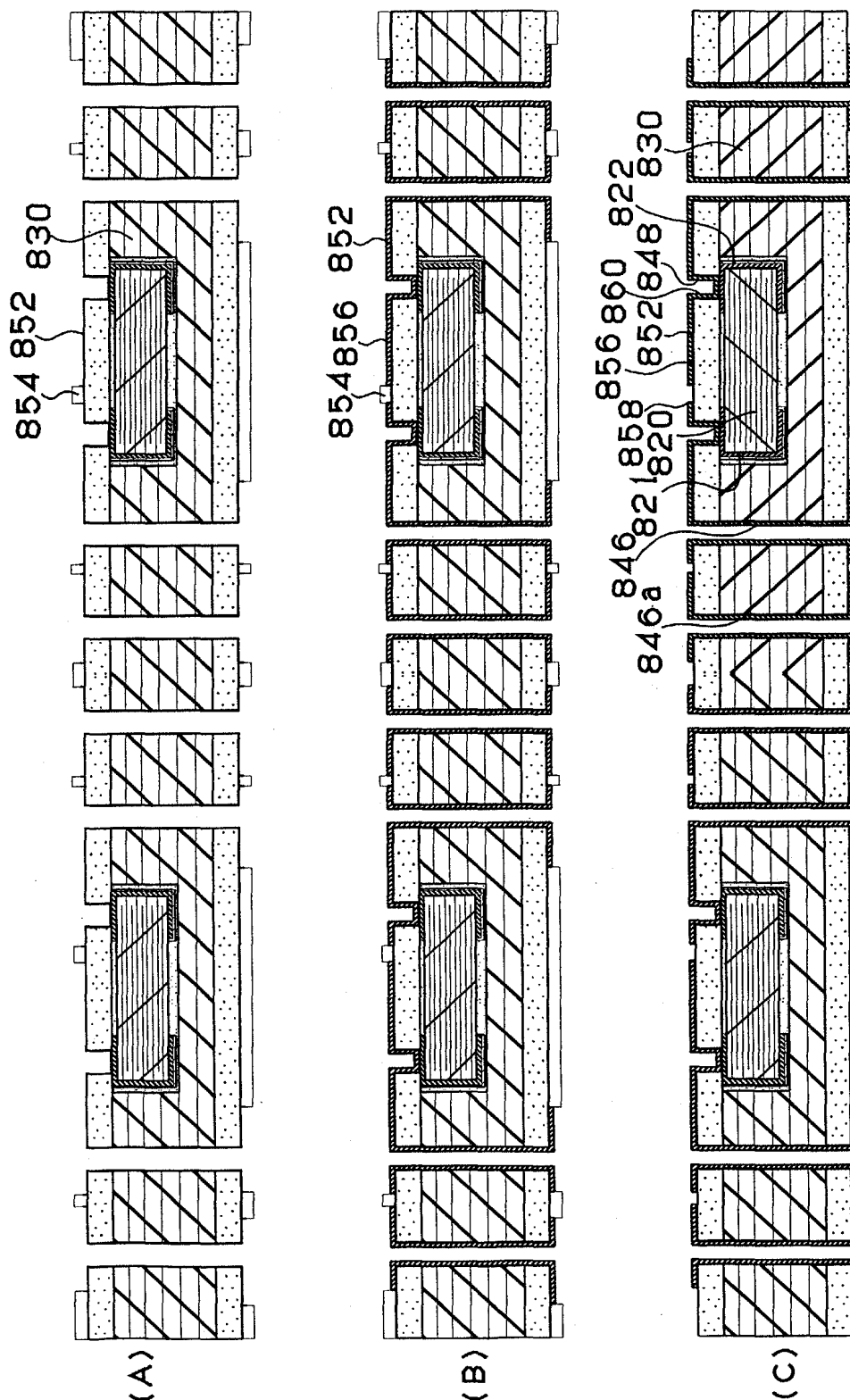
60/73  
Fig. 60



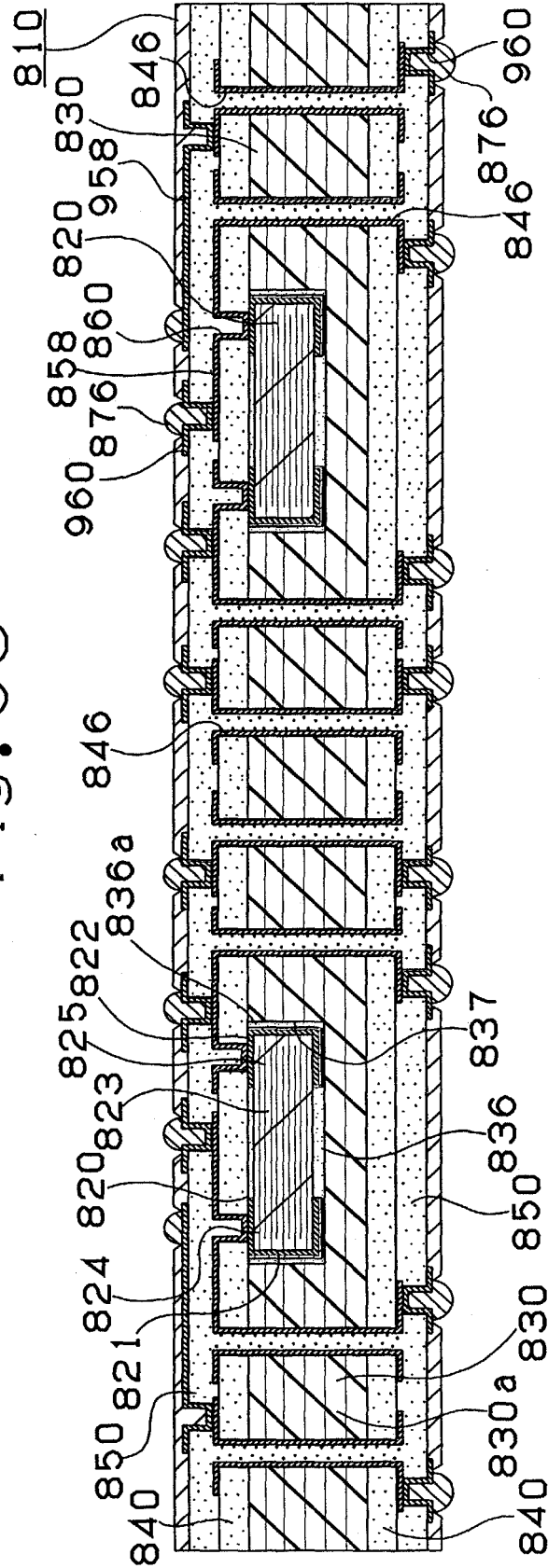
61/73  
Fig. 61



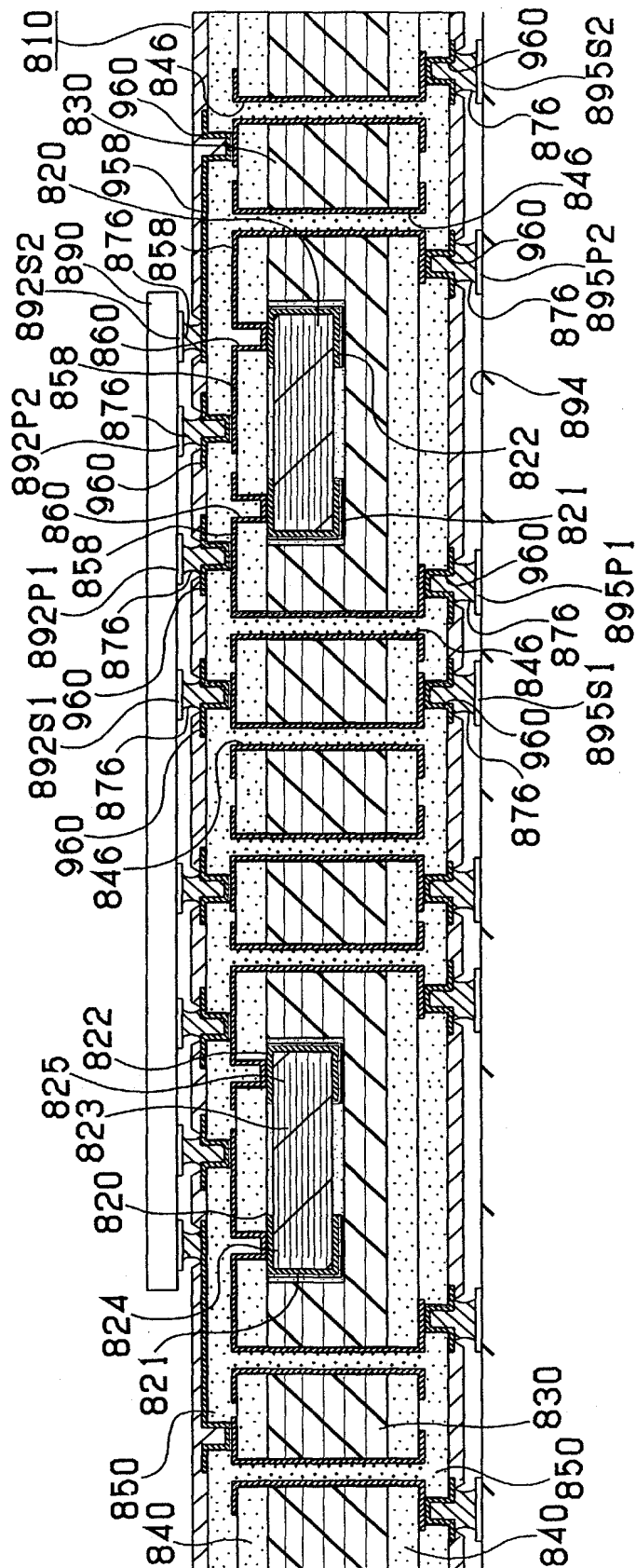
62/73  
Fig. 62



63/73  
Fig. 63

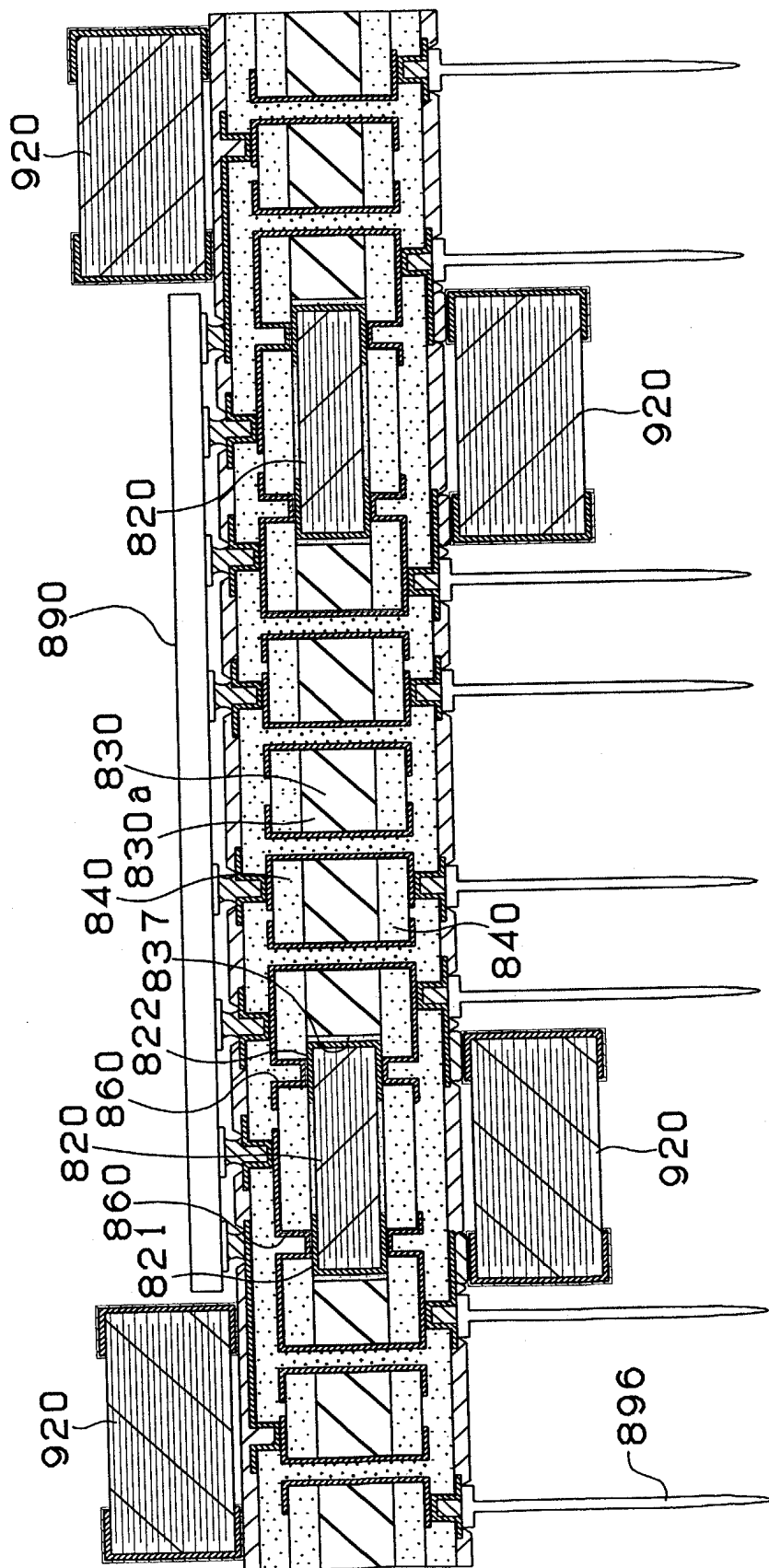


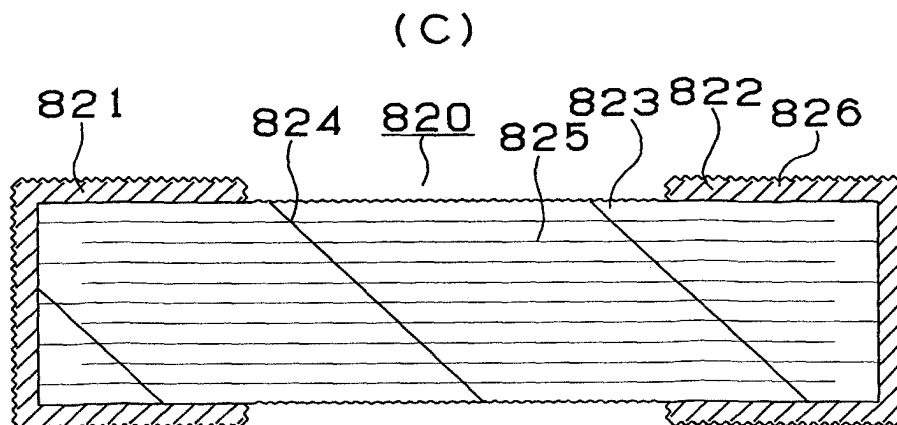
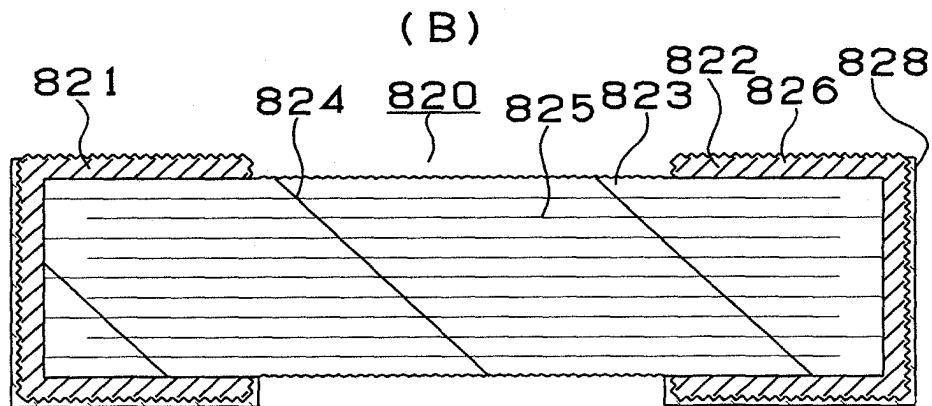
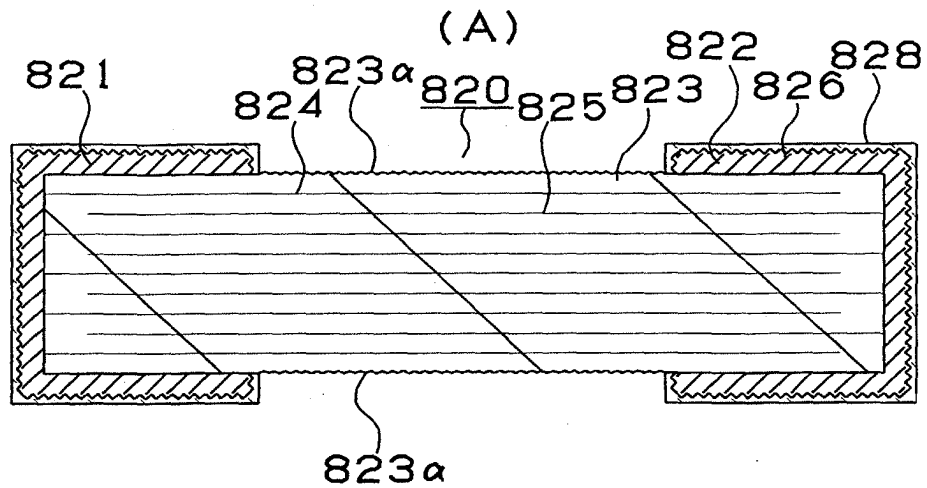
64/73  
Fig. 64



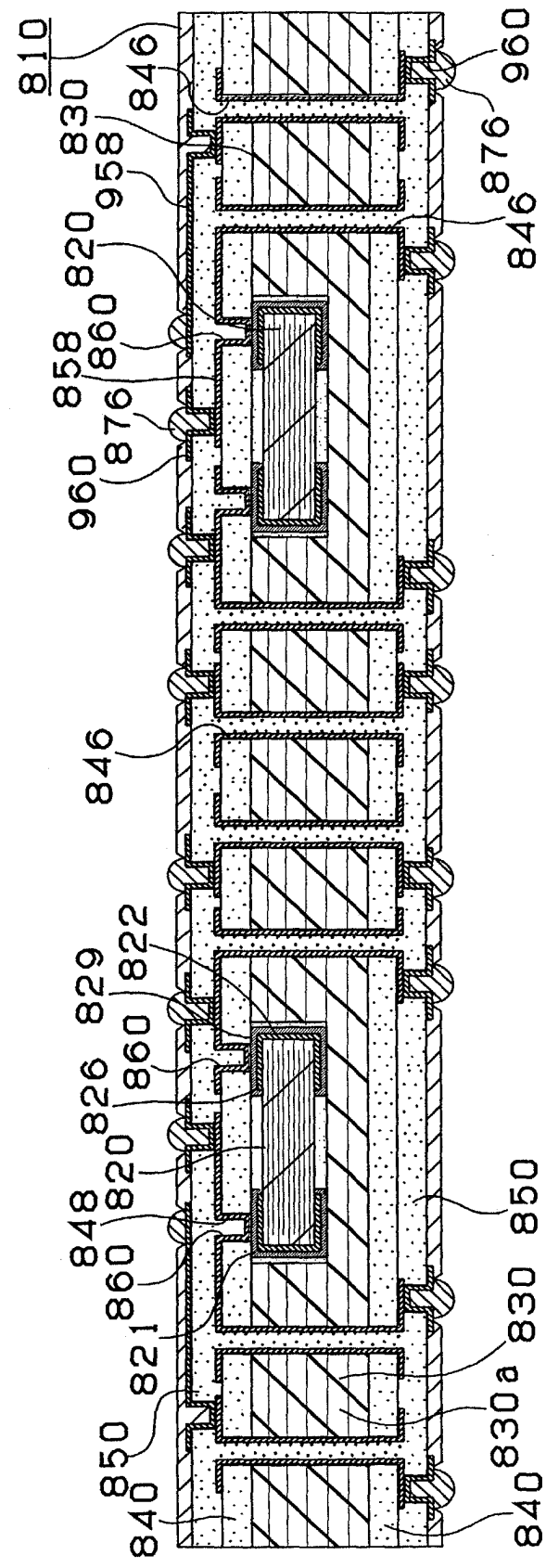


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Fig. 65



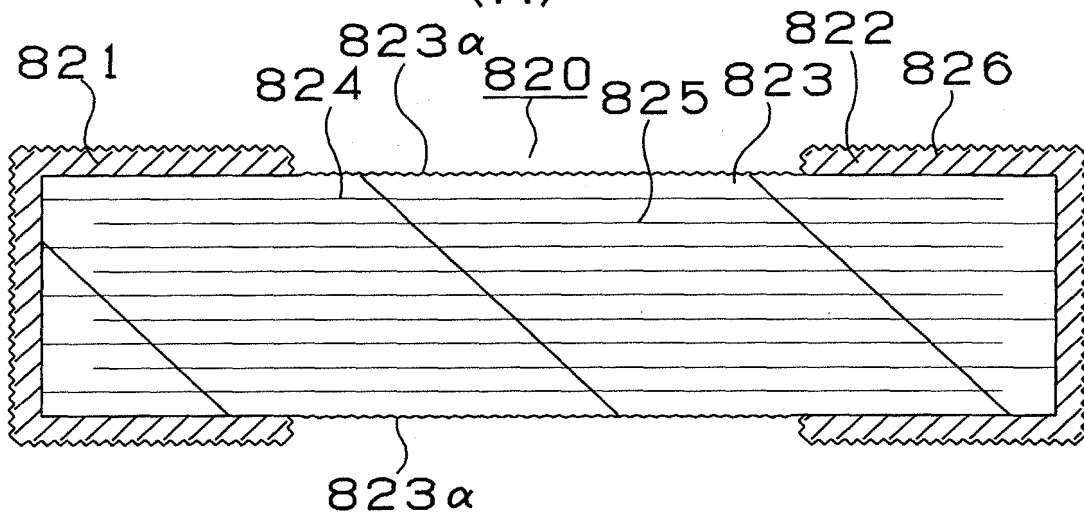
66/73  
Fig. 66

67/73  
Fig. 67

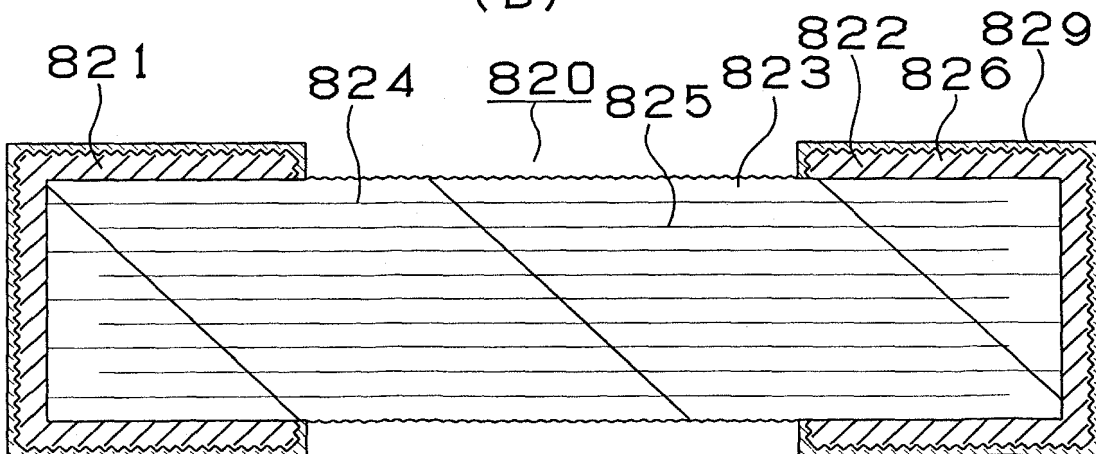


68/73  
Fig. 68

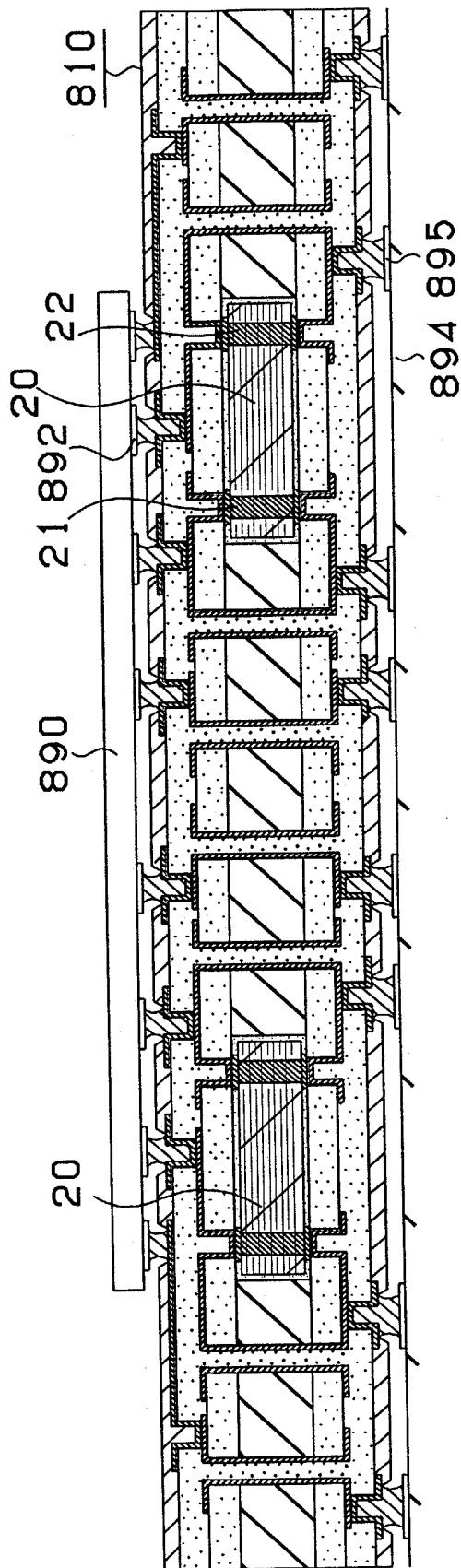
(A)



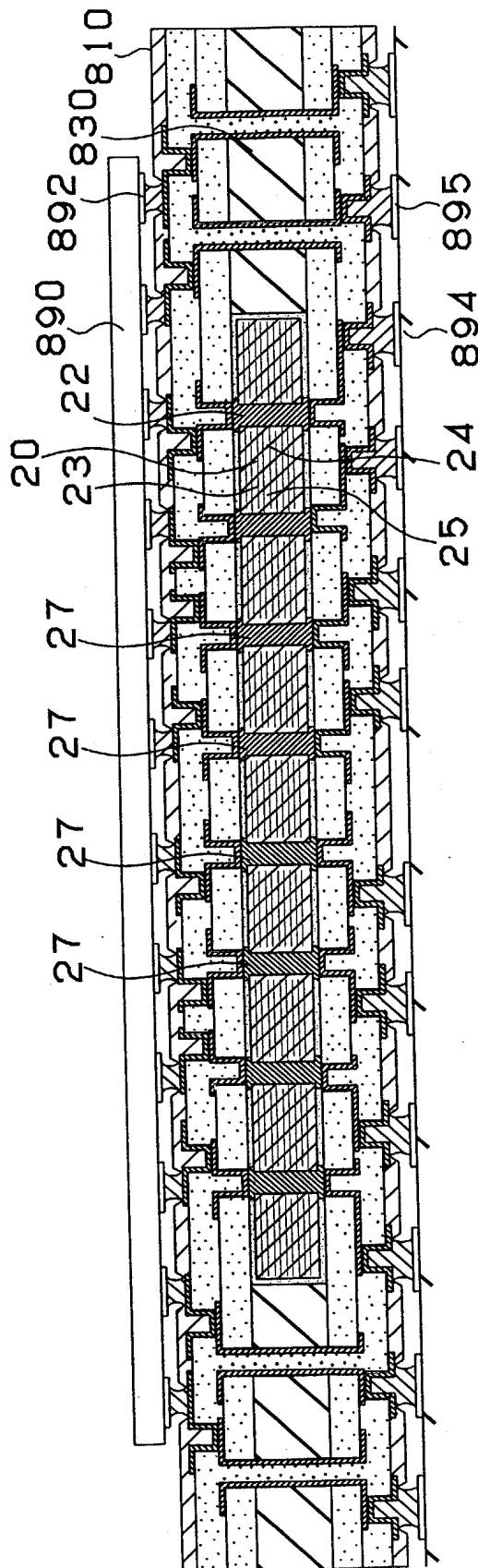
(B)



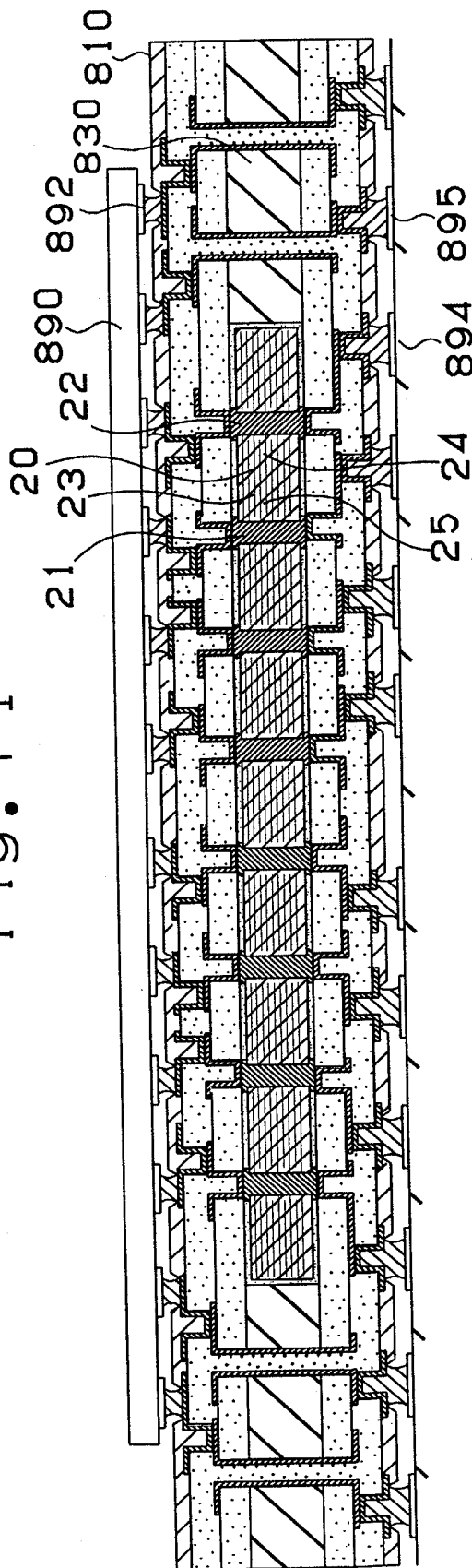
69/73  
Fig. 69



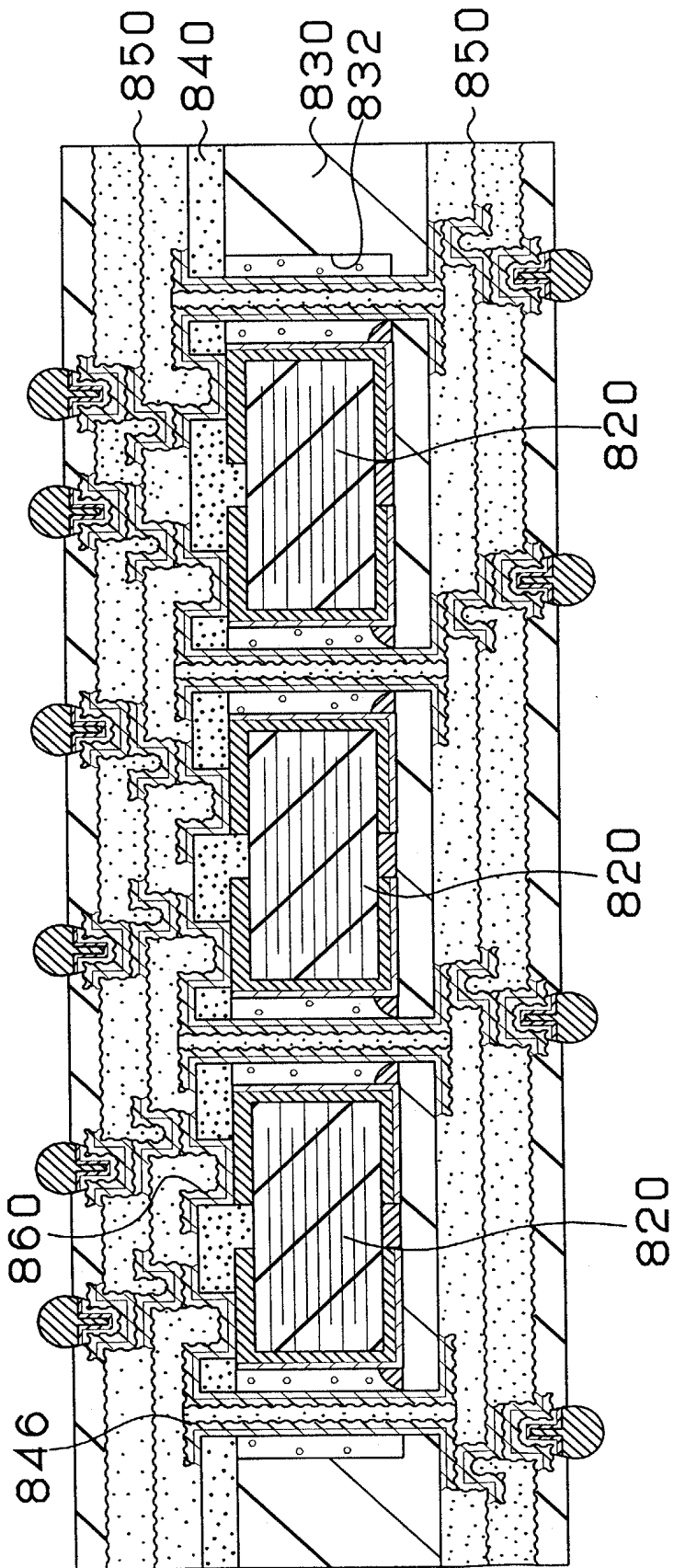
70/73  
Fig. 70



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Fig. 71



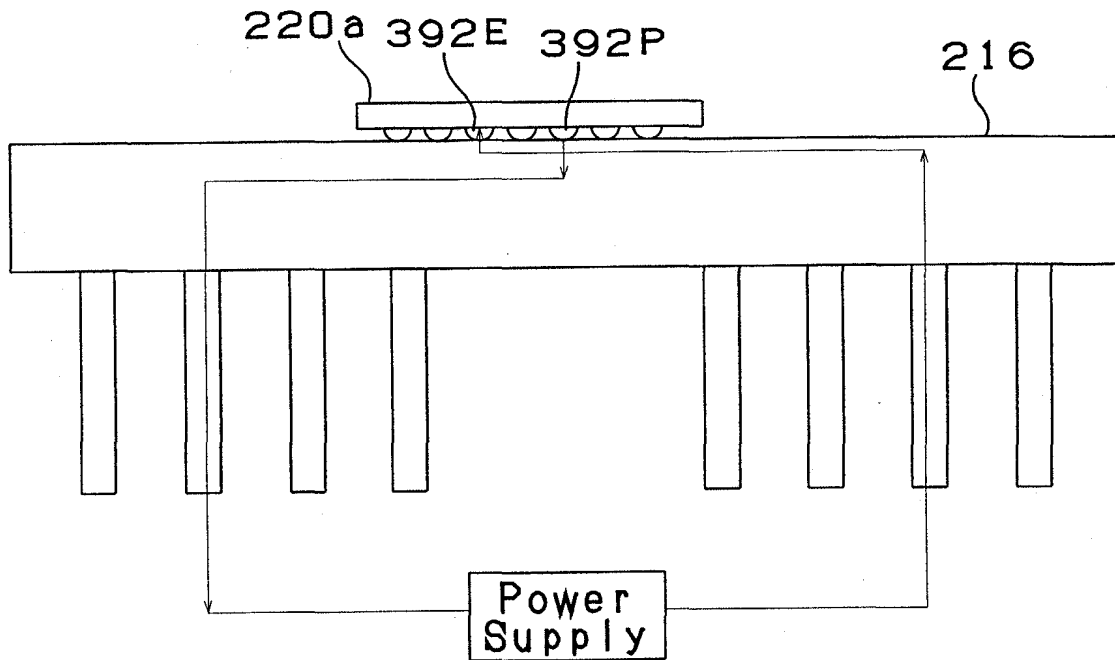
72/73  
Fig. 72





73/73  
Fig. 73

(A)



(B)

